

1. General description

Passivated thyristors in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance.

2. Features and benefits

- High blocking voltage suitable for high voltage applications
- High thermal cycling performance

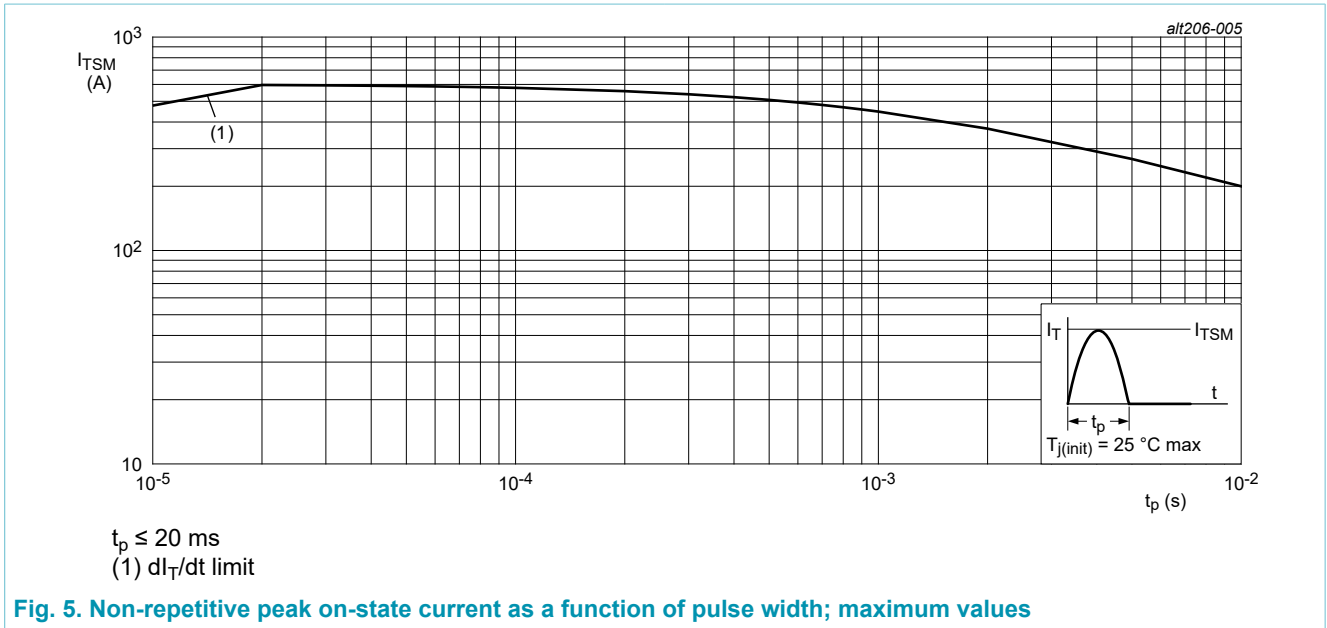
3. Applications

- General purpose switching
- Protection Circuits
- Motor control
- Industrial and domestic lighting

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
V_{RRM}	repetitive peak reverse voltage		-	-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 104\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	13	A
$I_{T(RMS)}$	RMS on-state current		-	-	20	A
I_{TSM}	non-repetitive peak on-state current	$T_{j(\text{init})} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	200	A
		$T_{j(\text{init})} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	-	220	A
T_j	junction temperature		-	-	125	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 7	-	3	32	mA
V_T	on-state voltage	$I_T = 40\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.45	1.75	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 100\text{ }\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	200	300	-	V/ μs



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6	-	-	1.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	minimum footprint, FR4 board	-	-	55	K/W

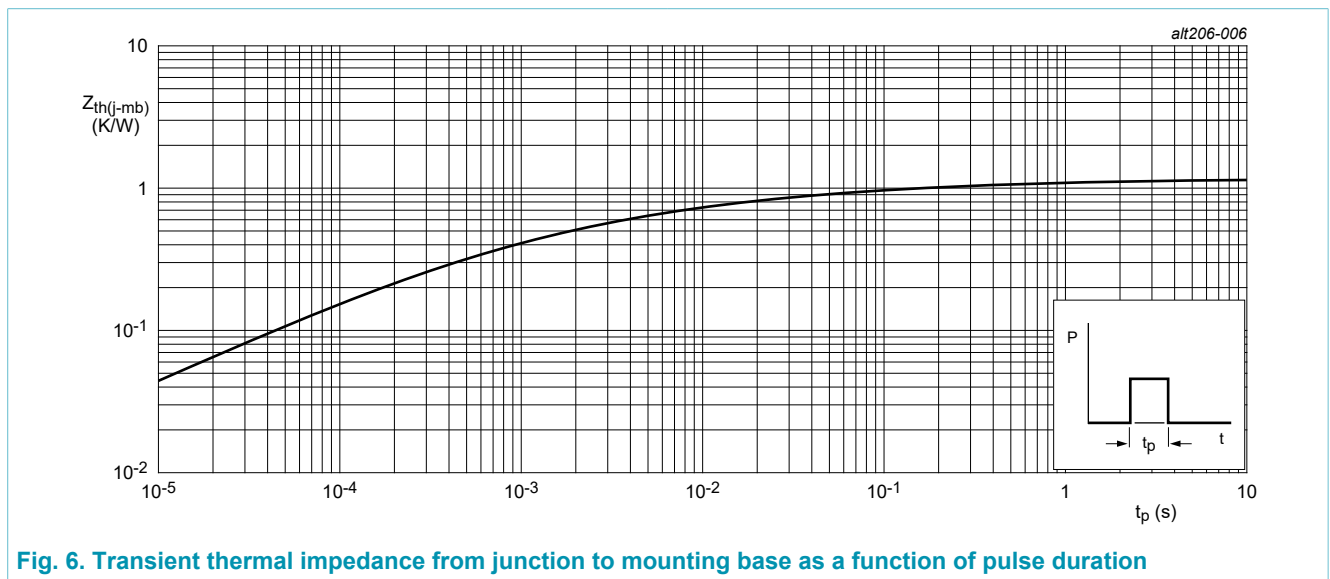


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 7	-	3	32	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 8	-	-	80	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	-	60	mA
V_T	on-state voltage	$I_T = 40\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.45	1.75	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	0.6	1.5	V
		$V_D = 800\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$; Fig. 11	0.25	0.4	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 125\text{ °C}$	-	0.2	1	mA
I_R	reverse current	$V_R = 800\text{ V}$; $T_j = 125\text{ °C}$	-	0.2	1	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 100\text{ }\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	200	300	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$I_{TM} = 40\text{ A}$; $V_D = 800\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$; $T_j = 25\text{ °C}$	-	2	-	μ s
t_q	commutated turn-off time	$V_{DM} = 800\text{ V}$; $T_j = 125\text{ °C}$; $I_{TM} = 50\text{ A}$; $V_R = 25\text{ V}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 50\text{ V}/\mu\text{s}$; $R_{GK(ext)} = 100\text{ }\Omega$; $V_{DM} = 67\%$ of V_{DRM}	-	70	-	μ s

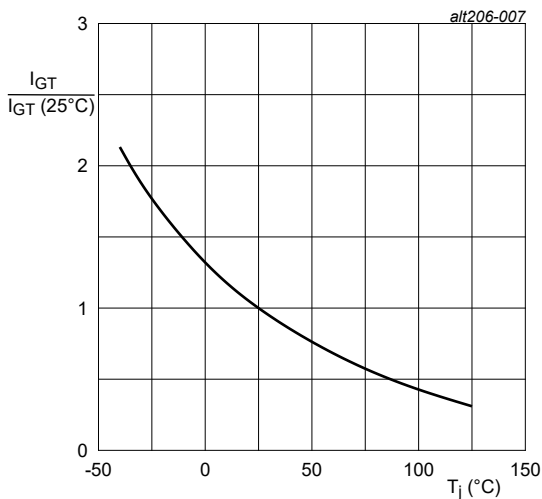


Fig. 7. Normalized gate trigger current as a function of junction temperature

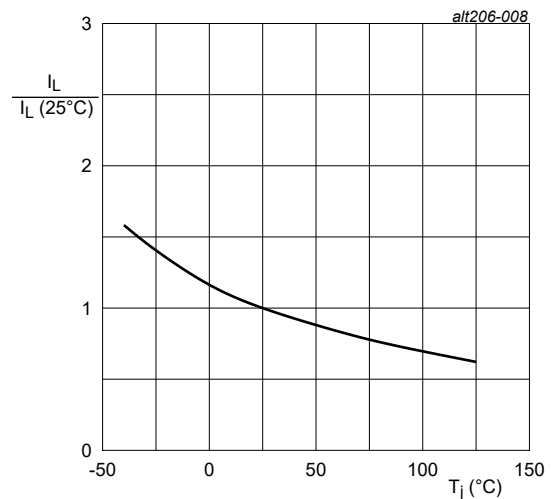


Fig. 8. Normalized latching current as a function of junction temperature

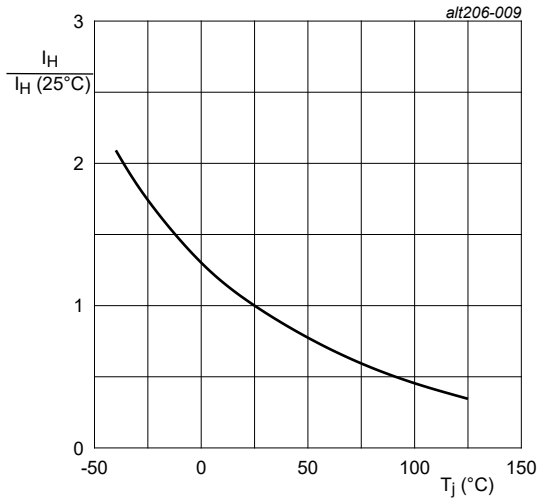
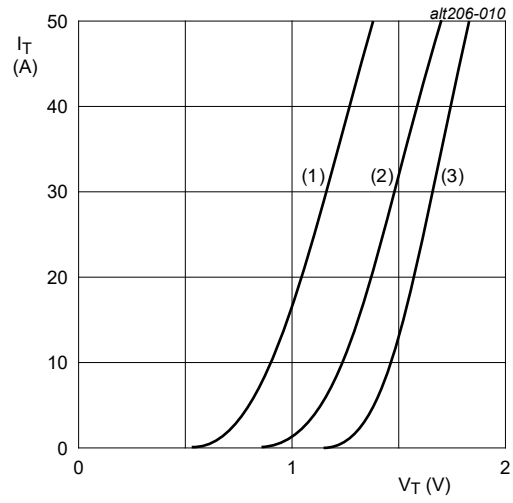


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.114 \text{ V}; R_s = 0.0125 \Omega$
 (1) $T_j = 125^\circ\text{C}$; typical values
 (2) $T_j = 125^\circ\text{C}$; maximum values
 (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

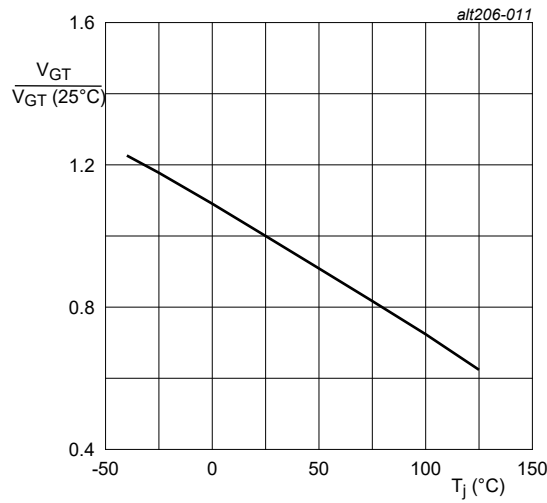


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) TO263

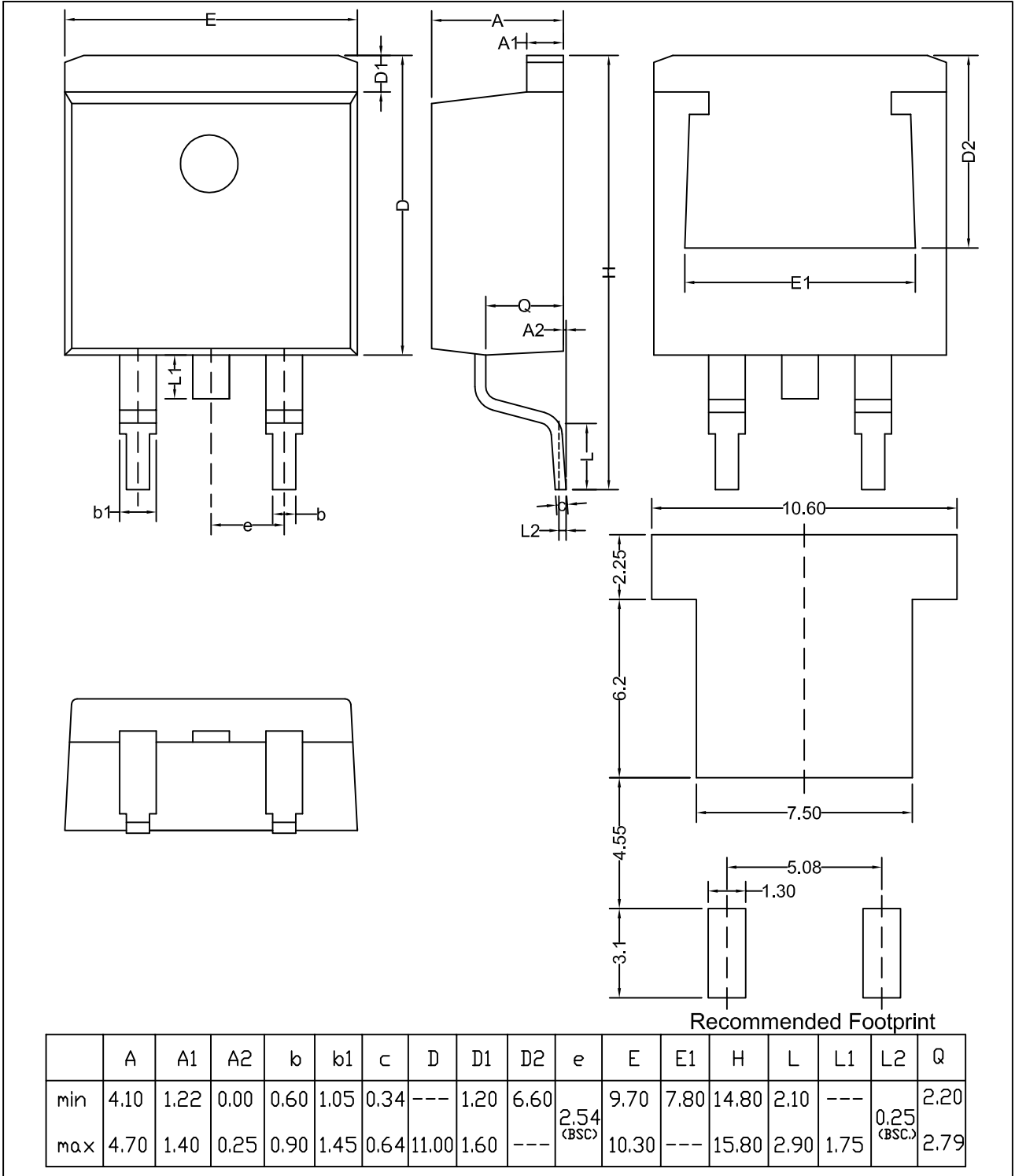


Fig. 12. Package outline D2PAK (SOT404)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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