**Product data sheet** 

## 1. General description

Planar passivated guaranteed commutation triac in a SOT223 surface mountable plastic package for use in motor control circuits or with other highly inductive loads. This triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers, including micro controllers.

### 2. Features and benefits

- · 3Q technology for improved noise immunity
- Direct triggering from low power drivers and logic ICs
- · High commutation capability with sensitive gate
- High immunity to false turn-on by dV/dt with sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Surface mountable package

## 3. Applications

- · General purpose motor controls
- Small loads in washing machines
- · Rectifier-fed DC inductive loads e.g. DC motors and solenoids

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DRM}$	repetitive peak off- state voltage		-	-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; $T_{sp} \le 108 ^{\circ}\text{C}$ ; Fig. 1; Fig. 2; Fig. 3	-	-	1	А
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 ^{\circ}C$ ; $t_p = 16.7  \text{ms}$	-	-	11	А
		full sine wave; $T_{j(init)} = 25 ^{\circ}\text{C}$ ; $t_p = 20  \text{ms}$ ; Fig. 4; Fig. 5	-	-	10	А
Tj	junction temperature		-	-	125	°C
Static characte	eristics					
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G+; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	-	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 9$	-	-	5	mA

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G-; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	-	5	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	-	6	mA
$V_{T}$	on-state voltage	I <sub>T</sub> = 2 A; T <sub>j</sub> = 25 °C; <u>Fig. 12</u>	-	1.2	1.5	V
Dynamic cha	racteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; $T_j$ = 125 °C; (67% of $V_{DRM}$ ); exponential waveform; gate open circuit	20	-	-	V/µs
dl <sub>com</sub> /dt	rate of change of commutating current	$V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 1 A; $dV_{com}/dt$ = 0.1 V/ $\mu$ s; gate open circuit	5	-	-	A/ms
		$V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 1 A; $dV_{com}/dt$ = 20 V/µs; (snubberless condition); gate open circuit	1	-	-	A/ms

# 5. Pinning information

#### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	4	T2—T1
2	T2	main terminal 2		G sym051
3	G	gate		Symost
4	mb	mounting base; connected to T2	⊟1 ⊟2 ⊟3 SC-73 (SOT223)	

# 6. Ordering information

### **Table 3. Ordering information**

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BTA204W-600D	SOT223	BTA204W-600D, 135	Reel	4000	SOT223	16-Mar-2006

Type number	Marking codes		
	Assembly factory: d	Assembly factory: L	
BTA204W-600D	Jdxxx 6D BTA204	JLxxx 6D BTA204	

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; $T_{sp} \le 108 ^{\circ}\text{C}$ ; Fig. 1; Fig. 2; Fig. 3	-	1	Α
I <sub>TSM</sub>	non-repetitive peak on-	full sine wave; $T_{j(init)} = 25  ^{\circ}C$ ; $t_p = 16.7  \text{ms}$	-	11	Α
	state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 20 \text{ ms}$ ; Fig. 4; Fig. 5	-	10	Α
l <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN	-	0.5	A²s
dl <sub>T</sub> /dt	rate of rise of on-state current	I <sub>G</sub> = 0.2 A	-	100	A/µs
I <sub>GM</sub>	peak gate current		-	1	Α
$P_{GM}$	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20ms period	-	0.5	W
T <sub>stg</sub>	storage temperature		-40	150	°C
Tj	junction temperature		-	125	°C

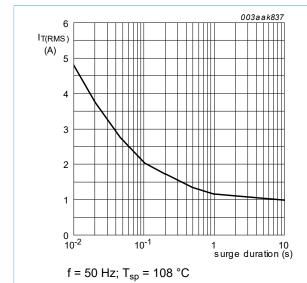


Fig. 1. RMS on-state current as a function of surge duration; maximum values

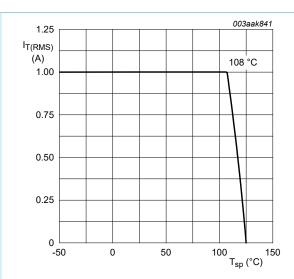


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values

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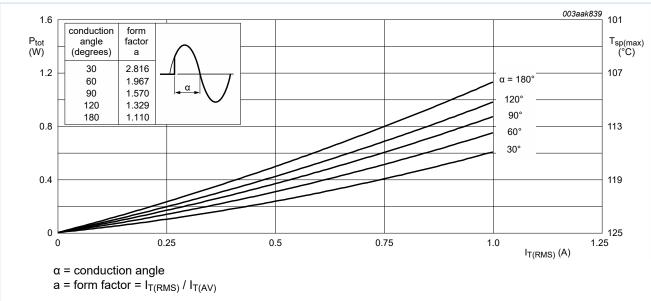


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

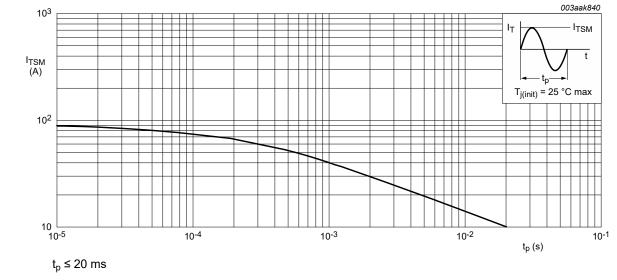


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

WeEn Semiconductors BTA204W-600D

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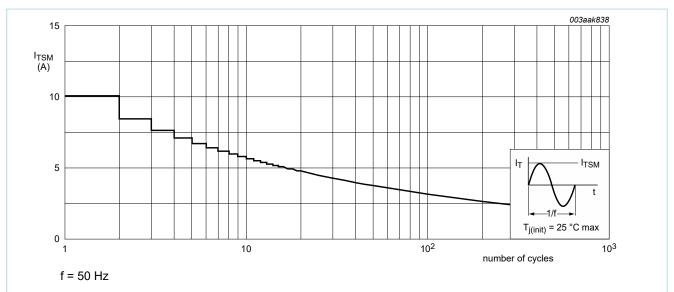


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

### 8. Thermal characteristics

**Table 5. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point	full cycle or half cycle; Fig. 6	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to	printed circuit board mounted: minimum pad area; Fig. 7	-	70	-	K/W
	ambient free air	printed circuit board mounted: minimum footprint; Fig. 8	-	156	-	K/W

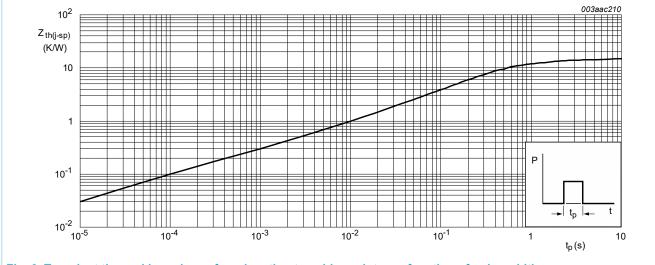
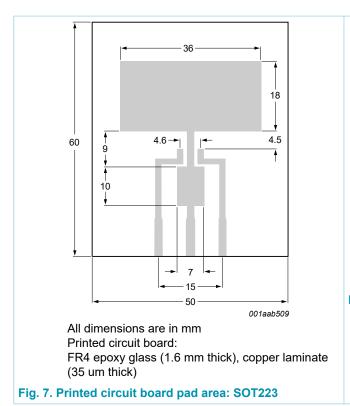


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width

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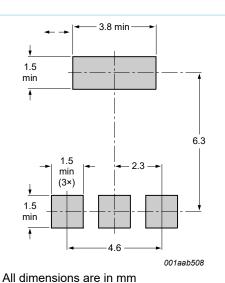


Fig. 8. Minimum footprint SOT223

## 9. Characteristics

#### **Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics	1			,	,
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 9$	-	-	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 9$	-	-	5	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; T2- G-;}$ $T_j = 25 \text{ °C; } Fig. 9$	-	-	5	mA
I <sub>L</sub> latching current	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 10$	-	-	6	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 10$	-	-	9	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 ^{\circ}\text{C}; \text{ Fig. 10}$	-	-	6	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	-	6	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 2 A; T <sub>j</sub> = 25 °C; <u>Fig. 12</u>	-	1.2	1.5	V
$V_{GT}$	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 13	-	0.7	1	V
		$V_D = 400 \text{ V}; I_T = 0.1 \text{ A}; T_j = 125 ^{\circ}\text{C};$ Fig. 13	0.25	0.4	-	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 125 °C	-	0.1	0.5	mA
Dynamic cl	naracteristics		'			,
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; $T_j$ = 125 °C; (67% of $V_{DRM}$ ); exponential waveform; gate open circuit	20	-	-	V/µs
dl <sub>com</sub> /dt	rate of change of commutating current	$V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 1 A; $dV_{com}/dt$ = 0.1 V/ $\mu$ s; gate open circuit	5	-	-	A/ms
		$V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 1 A; $dV_{com}/dt$ = 20 V/µs; (snubberless condition); gate open circuit	1	-	-	A/ms

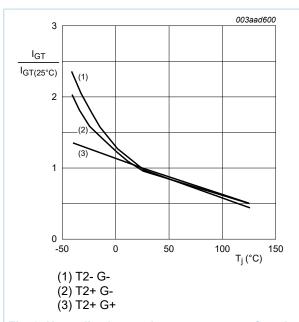


Fig. 9. Normalized gate trigger current as a function of junction temperature

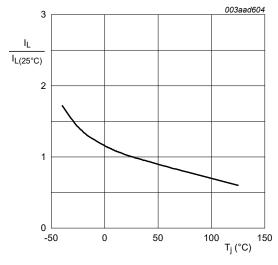


Fig. 10. Normalized latching current as a function of junction temperature

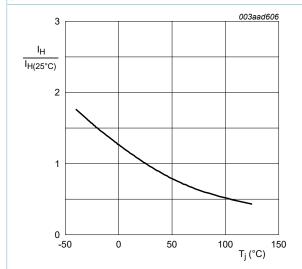
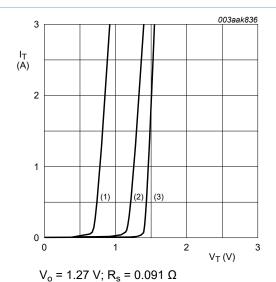


Fig. 11. Normalized holding current as a function of junction temperature

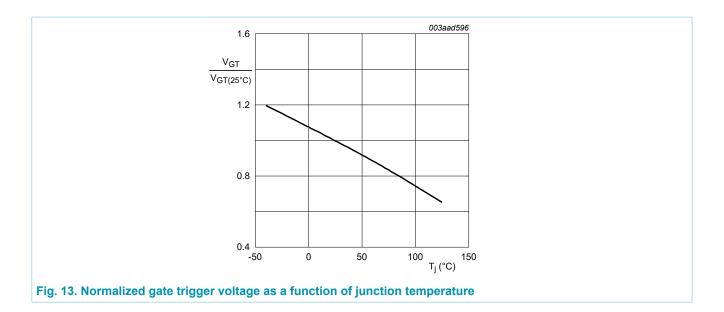


(1)  $T_j = 125$  °C; typical values (2)  $T_j = 125$  °C; maximum values (3)  $T_j = 25$  °C; maximum values

Fig. 12. On-state current as a function of on-state voltage

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## 10. Package outline

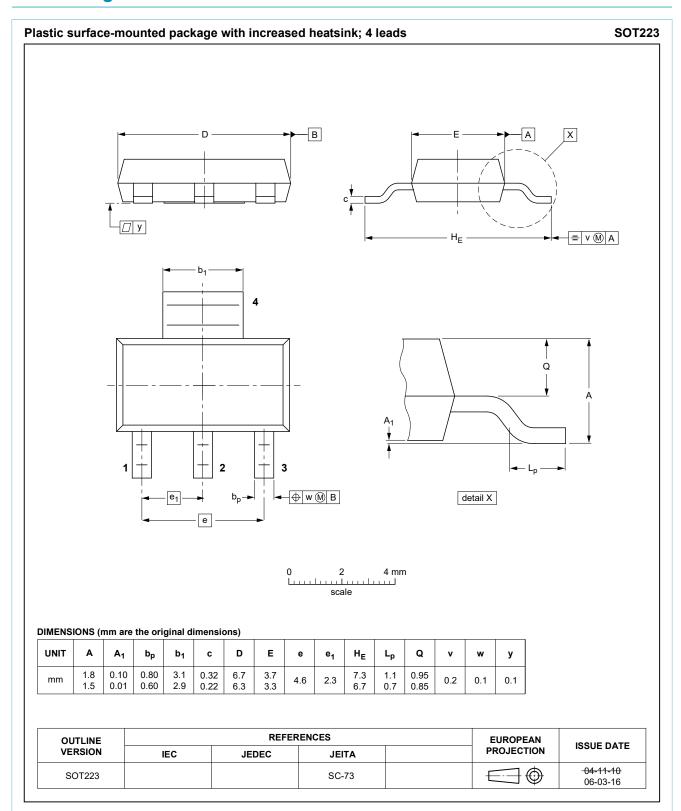


Fig. 14. Package outline SC-73 (SOT223)

## 11. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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For more information, please visit: http://www.ween-semi.com
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