DATA SHEET

BTA212B series B
Three quadrant triacs
high commutation

Product specification

September 2019

WeEn
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Three quadrant triacs high commutation

BTA212B series B

GENERAL DESCRIPTION

Planar passivated high commutation triacs in a plastic envelope suitable for surface mounting intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

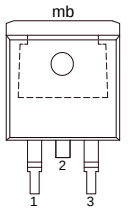
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BTA212B-	**500B**	**600B**	**800B**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
I_{TSM}	Non-repetitive peak on-state current	95	95	95	A

PINNING - SOT404

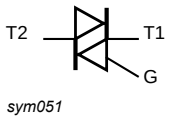
PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
mb	main terminal 2

PIN CONFIGURATION



D2PAK (SOT404)

SYMBOL



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LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	**-600**	**-800**	
V_{DRM}	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 99$ ˚C	-	12			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ ˚C prior to surge					
		t = 20 ms	-	95			A
		t = 16.7 ms	-	105			A
I^2t	I^2t for fusing	t = 10 ms	-	45			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 20 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs		100			A/µs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	125			˚C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	1.5	K/W
		half cycle	-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A					
			T2+ G+	2	18	50	mA
			T2+ G-	2	21	50	mA
			T2- G-	2	34	50	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A					
			T2+ G+	-	31	60	mA
			T2+ G-	-	34	90	mA
			T2- G-	-	30	60	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A		-	31	60	mA
V_T	On-state voltage	I_T = 17 A		-	1.3	1.6	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A		-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C		0.25	0.4	-	V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C		-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	1000	4000	-	V/µs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 12 A; without snubber; gate open circuit	-	24	-	A/ms
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

2 Device does not trigger in the T2-, G+ quadrant.

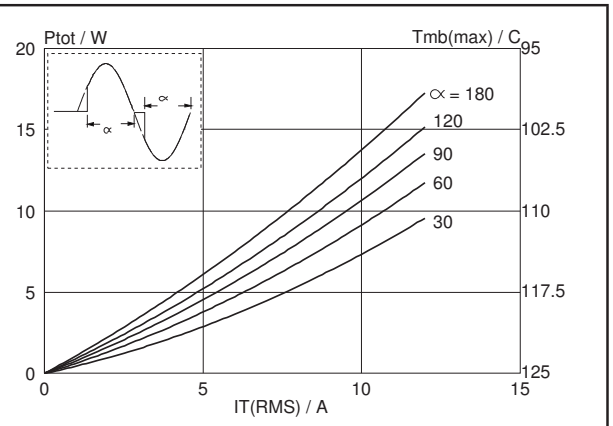


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

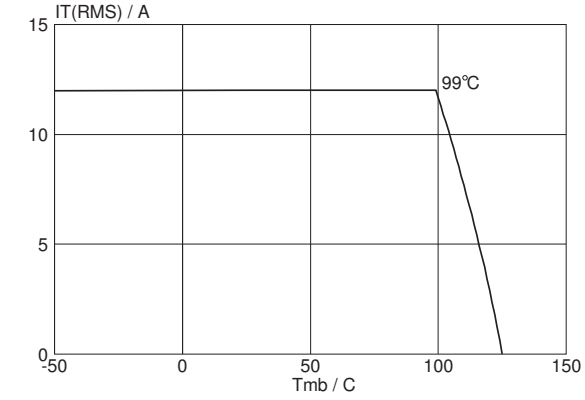


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

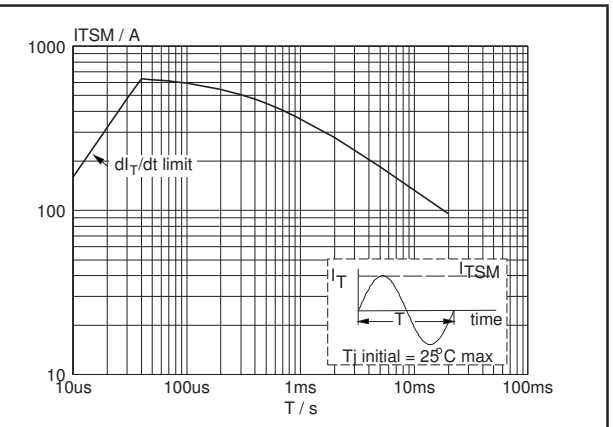


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

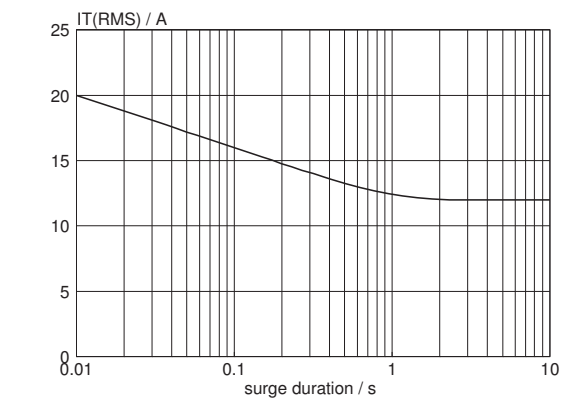


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 99˚C$.

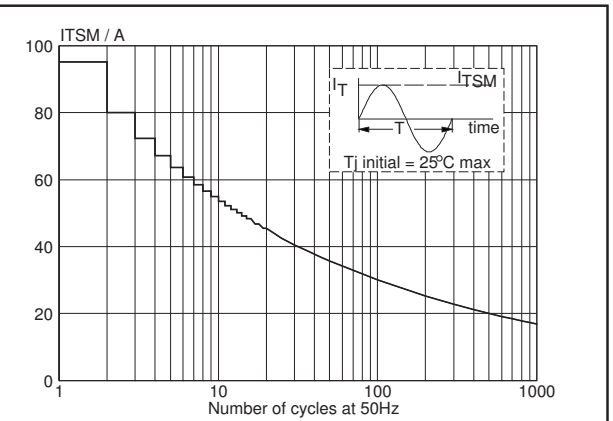


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

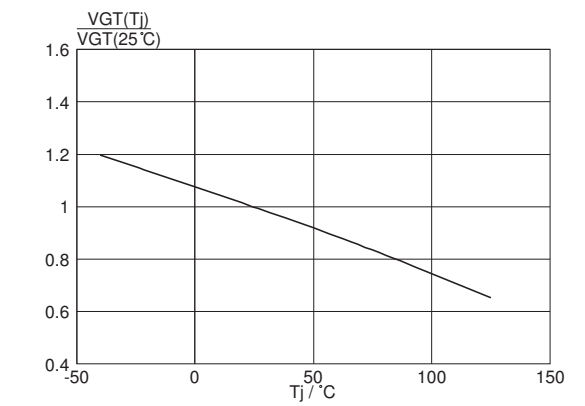


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25˚C)$, versus junction temperature T_j.

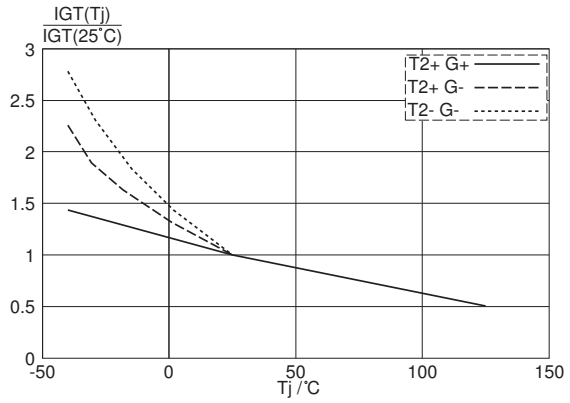


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25˚C)$, versus junction temperature T_j.

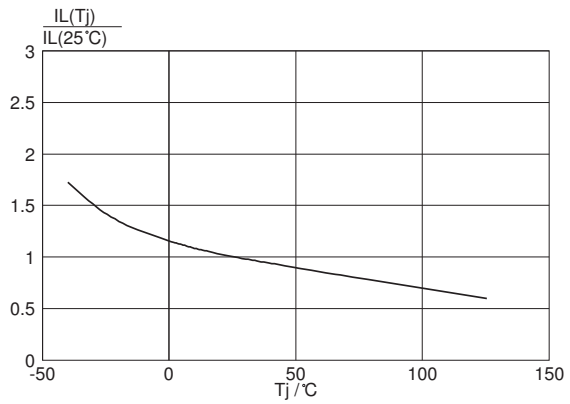


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25˚C)$, versus junction temperature T_j.

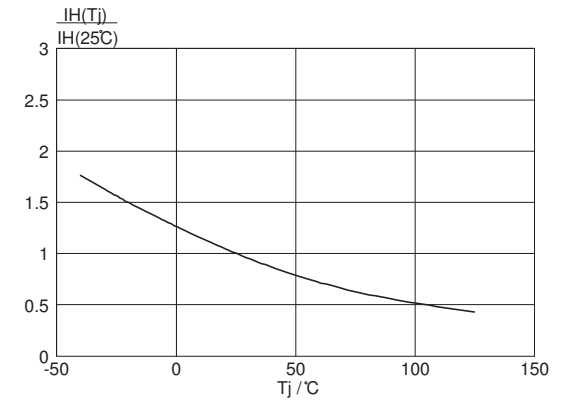


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25˚C)$, versus junction temperature T_j.

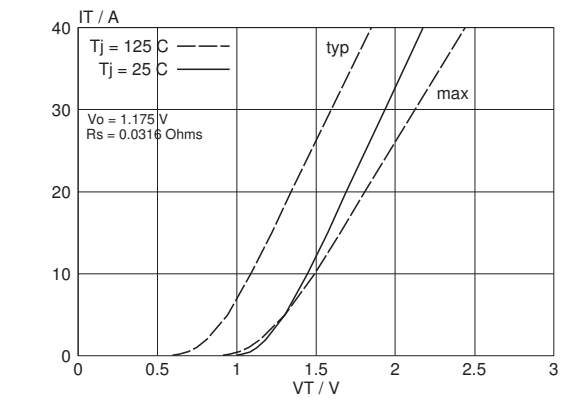


Fig.10. Typical and maximum on-state characteristic.

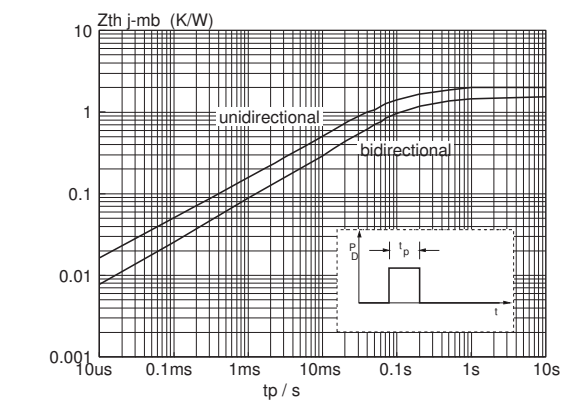


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

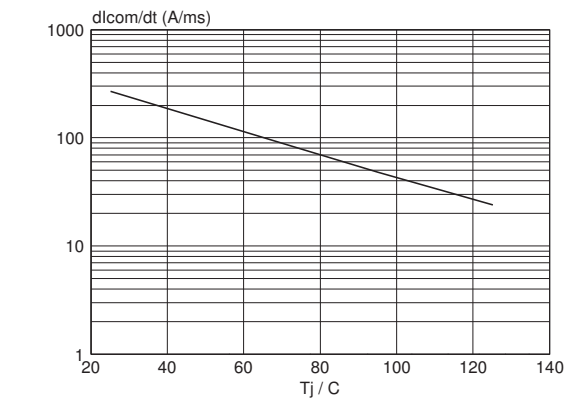
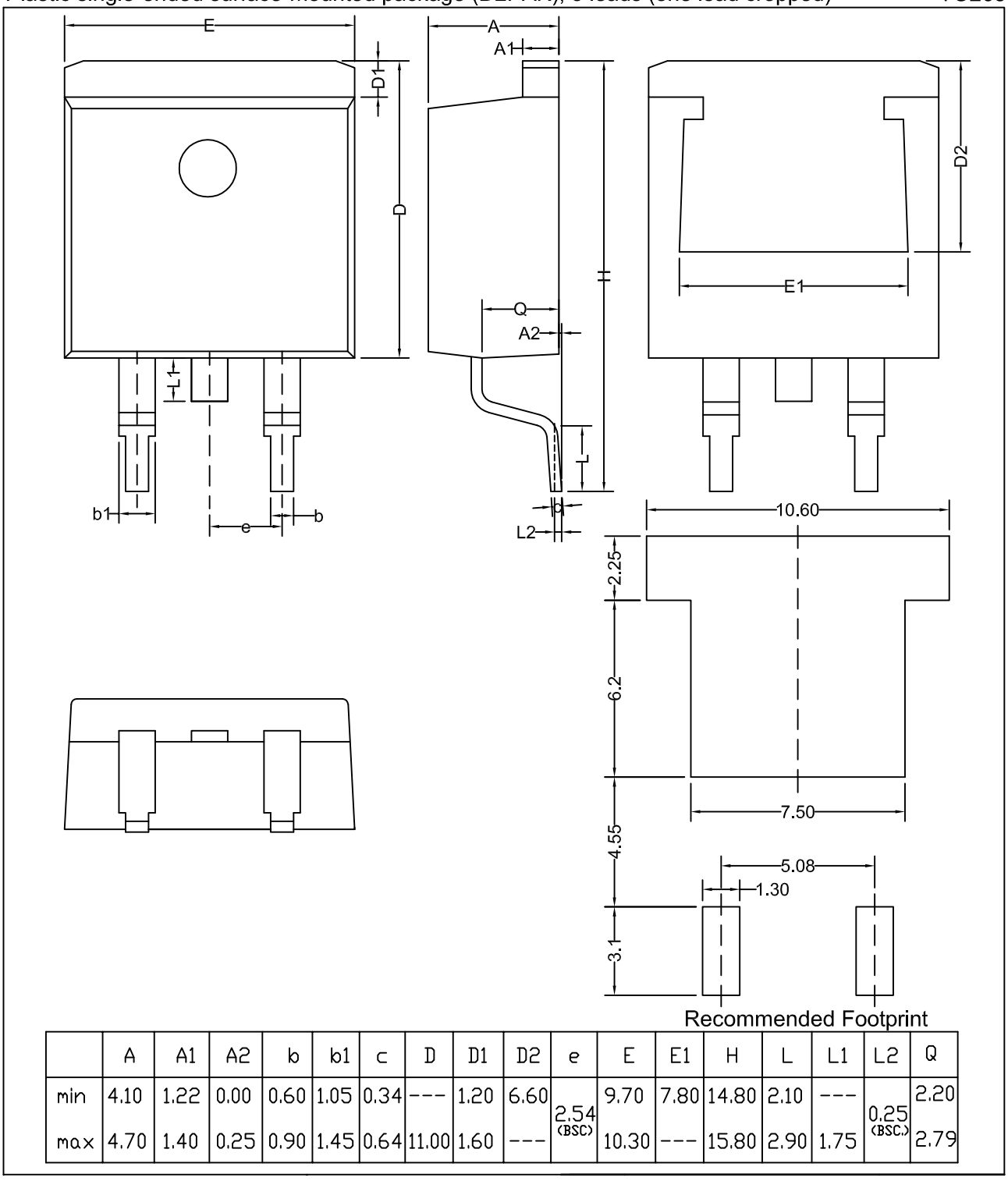


Fig.12. Typical, critical rate of change of commutating current dI_{com}/dt versus junction temperature.

MECHANICAL DATA

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) TO263



	A	A1	A2	b	b1	c	D	D1	D2	e	E	E1	H	L	L1	L2	Q
min	4.10	1.22	0.00	0.60	1.05	0.34	---	1.20	6.60	2.54 (BSC)	9.70	7.80	14.80	2.10	---	0.25 (BSC)	2.20
max	4.70	1.40	0.25	0.90	1.45	0.64	11.00	1.60	---		10.30	---	15.80	2.90	1.75		2.79

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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