

**Product data sheet** 

#### **1. General description**

Planar passivated very sensitive gate four quadrant triac in a TO92 plastic package intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

#### 2. Features and benefits

- Direct interfacing to logic level ICs
- · Direct interfacing to low power gate drivers and microcontrollers
- High blocking voltage capability
- · Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

### 3. Applications

- · General purpose low power phase control
- General purpose low power switching
- Solid-state relay

### 4. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Absolute	maximum rating	· ·	I			
$V_{\text{DRM}}$	repetitive peak off-state voltage		-	-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; T <sub>lead</sub> ≤ 50 °C; <u>Fig. 1;</u> <u>Fig. 2; Fig. 3</u>	-	-	0.6	A
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5	-	-	8	A
		full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.7 ms	-	-	8.8	А
Tj	junction temperature		-	-	125	°C
Static ch	aracteristics	· ·	I			
I <sub>GT</sub>	gate trigger current	$V_{D} = 12 \text{ V}; \text{ I}_{T} = 0.1 \text{ A}; \text{ T2+ G+};$ T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	1	5	mA
		$V_{D} = 12 \text{ V}; \text{ I}_{T} = 0.1 \text{ A}; \text{ T2+ G-};$ T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	2	5	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G-; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	2	5	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G+; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	4	7	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	1	10	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 0.85 A; T <sub>i</sub> = 25 °C; <u>Fig. 10</u>	-	1.4	1.9	V

4Q Triac

**MAC97A8** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Dynamic characteristics							
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; T <sub>j</sub> = 110 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit; Fig. 12		30	45	-	V/µs
dV <sub>com</sub> /dt	rate of change of commutating voltage	$V_D = 600 \text{ V}; \text{ T}_j = 50 \text{ °C}; \text{ dI}_{com}/\text{dt} = 0.3 \text{ A/ms};$ I <sub>T</sub> = 0.84 A; gate open circuit		-	5	-	V/µs

# 5. Pinning information

Table 2. P	able 2. Pinning information							
Pin	Symbol	Description	Simplified outline	Graphic symbol				
1	T2	main terminal 2		N I				
2	G	gate		T2-T1				
3	T1	main terminal 1	() (	sym051				

## 6. Ordering information

Table 3. Ordering info	ormation					
Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
MAC97A8	TO92	MAC97A8,412	Bulk	1000	SOT54	14-Nov-2013
MAC97A8	TO92	MAC97A8,116	Reel	2000	SOT54 wide pitch	14-Nov-2013
MAC97A8/DG	TO92	MAC97A8/DG,412	Bulk	1000	SOT54	14-Nov-2013
MAC97A8/DG	TO92	MAC97A8/DG,116	Reel	2000	SOT54 wide pitch	14-Nov-2013

## 7. Marking

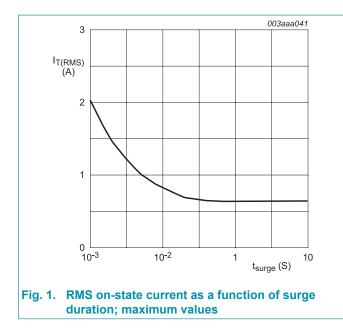
Table 4. Marking codes	
Type number	Marking codes
MAC97A8	MAC97A8

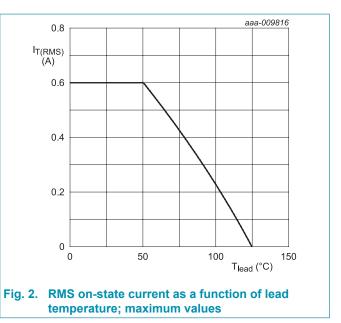
# 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

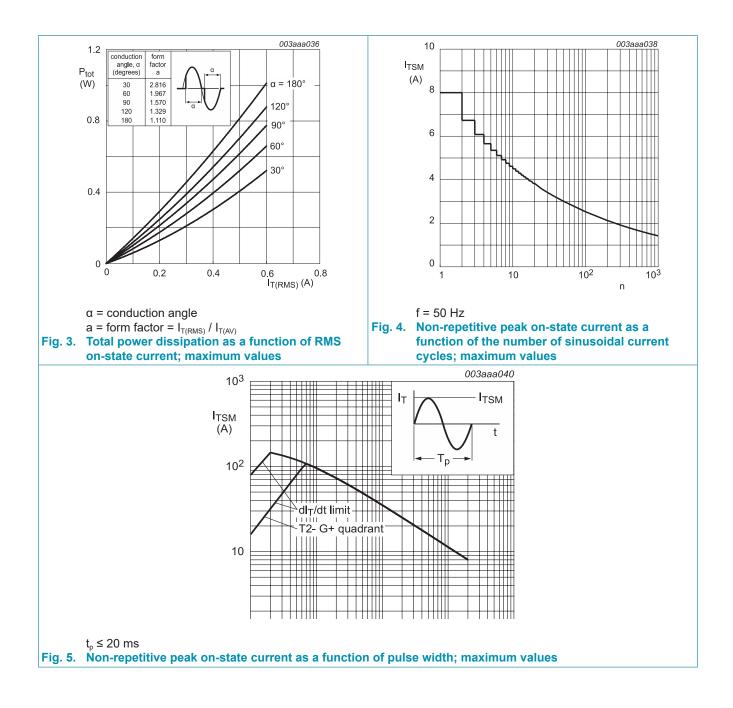
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{\text{DRM}}$	repetitive peak off-state voltage		-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; T <sub>lead</sub> ≤ 50 °C; <u>Fig 1</u> ; <u>Fig 2</u> ; <u>Fig 3</u>	-	0.6	A
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig 4; Fig 5	-	8	A
		full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.7 ms	-	8.8	А
l <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; sine-wave pulse	-	0.32	A <sup>2</sup> s
1.	rate of rise of on-state current	I <sub>G</sub> = 20 mA; T2+ G+	-	50	A/µs
		I <sub>G</sub> = 20 mA; T2+ G-	-	50	A/µs
		I <sub>G</sub> = 20 mA; T2- G-	-	50	A/µs
		I <sub>G</sub> = 20 mA; T2- G+	-	10	A/µs
I <sub>GM</sub>	peak gate current		-	1	А
P <sub>GM</sub>	peak gate power		-	5	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period	-	0.1	W
T <sub>stg</sub>	storage temperature		-40	150	°C
T <sub>i</sub>	junction temperature		-	125	°C





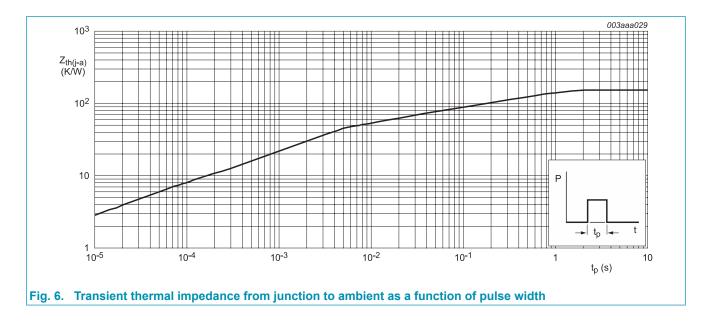
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### 9. Thermal characteristics

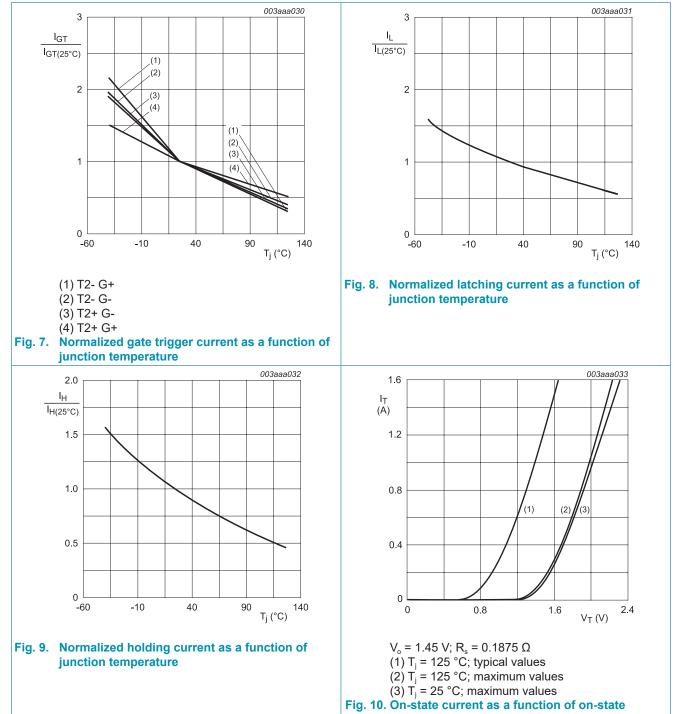
Table 6. Th	ermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-lead)}$	thermal resistance	full cycle; <u>Fig 6</u>	-	-	60	K/W
	from junction to lead	half cycle	-	-	80	K/W
$R_{\text{th(j-a)}}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



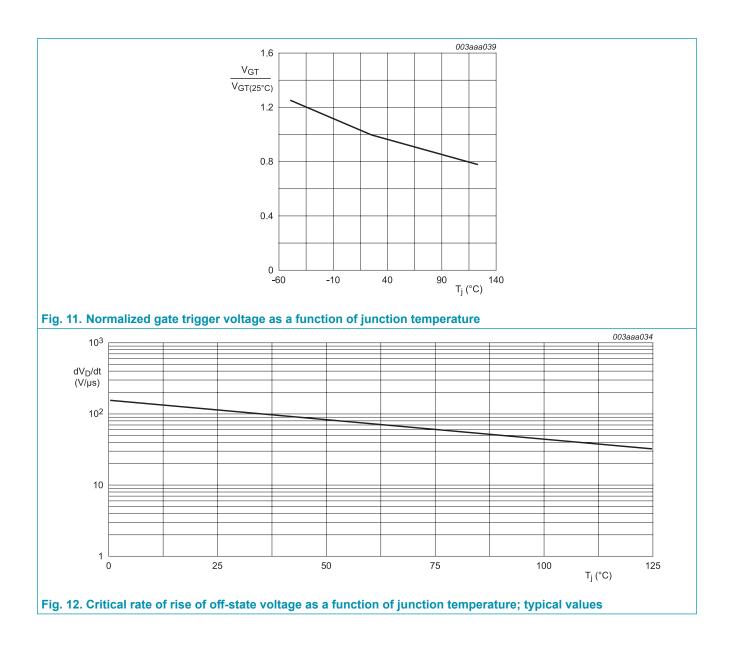
## **10. Characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	aracteristics	1				
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; \text{ I}_T = 0.1 \text{ A}; \text{ T2+ G+};$ $T_j = 25 \text{ °C}; \text{ Fig. 7}$	-	1	5	mA
GT GT L L V T VGT D D D D D D D D D D D D D D D D D D D		$V_{D} = 12 \text{ V}; \text{ I}_{T} = 0.1 \text{ A}; \text{ T2+ G-};$ $T_{j} = 25 \text{ °C}; \text{ Fig. 7}$	-	2	5	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G-; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	2	5	mA
		$V_{D} = 12 \text{ V}; \text{ I}_{T} = 0.1 \text{ A}; \text{ T2- G+};$ T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	4	7	mA
I <sub>L</sub>	latching current	$V_{D} = 12 \text{ V}; \text{ I}_{G} = 0.1 \text{ A}; \text{ T2+ G+};$ T <sub>j</sub> = 25 °C; <u>Fig. 8</u>	-	1	10	mA
		$V_{D}$ = 12 V; I <sub>G</sub> = 0.1 A; T2+ G-; T <sub>j</sub> = 25 °C; <u>Fig. 8</u>	-	5	10	mA
		$V_{D} = 12 \text{ V}; \text{ I}_{G} = 0.1 \text{ A}; \text{ T2- G-};$ T <sub>j</sub> = 25 °C; <u>Fig. 8</u>	-	1	10	mA
		$V_{D}$ = 12 V; I <sub>G</sub> = 0.1 A; T2- G+; T <sub>j</sub> = 25 °C; <u>Fig. 8</u>	-	2	10	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	1	10	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 0.85 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.4	1.9	V
V <sub>GT</sub>	gate trigger voltage	$V_D = 12 \text{ V}; \text{ I}_T = 0.1 \text{ A}; \text{ T}_j = 25 \text{ °C};$ Fig. 11	-	0.9	1.5	V
I <sub>H</sub> V <sub>T</sub> V <sub>GT</sub> I <sub>D</sub> Dynamic cł		V <sub>D</sub> = 400 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 110 °C	0.1	0.7	-	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 110 °C	-	3	100	μA
Dynamic	characteristics		I			
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM} = 402 \text{ V}; \text{ T}_{j} = 110 \text{ °C}; (V_{DM} = 67\% \text{ of } V_{DRM}); exponential waveform; gate open circuit; Fig. 12$	30	45	-	V/µs
dV <sub>com</sub> /dt	rate of change of commutating voltage	$V_D = 600 \text{ V}; \text{ T}_j = 50 \text{ °C}; \text{ dI}_{com}/\text{dt} = 0.3 \text{ A}/\text{ms}; \text{ I}_T = 0.84 \text{ A}; \text{ gate open circuit}$	-	5	-	V/µs
t <sub>gt</sub>	gate-controlled turn-on time	$I_{TM}$ = 1 A; $V_{\rm D}$ = 600 V; $I_{\rm G}$ = 25 mA; $dI_{\rm G}/$ $dt$ = 5 A/µs	-	2	-	μs

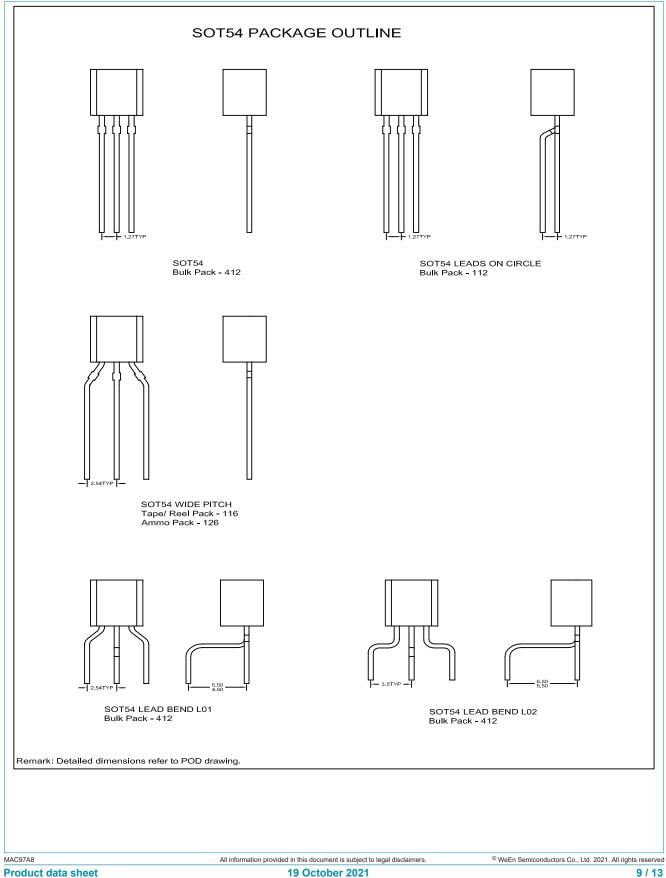
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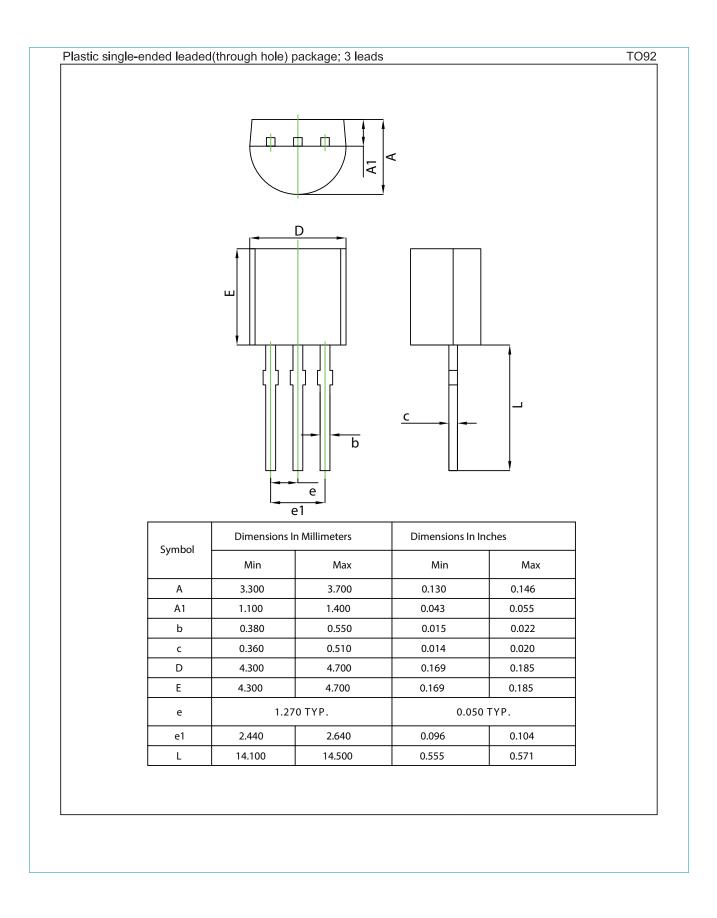


#### voltage



## 11. Package outline





## 12. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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	Features and benefits

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