1. Introduction

Datasheets are not required to be created to a fixed international standard. This means datasheets must be read and interpreted carefully to ensure that parameter descriptions and values are correctly understood.

This datasheet note looks at how the data values in WeEn datasheets are assured.

For understanding of parameter definitions, this note should be read alongside WeEn datasheet notes, WDN003, "Understanding the Triac Datasheet" and WDN004, "Understanding the SCR Datasheet"

2. How data values in WeEn datasheets are assured

The parameters for WeEn datasheets are assured in several ways: -

- Some parameters are assured by testing by calibrated Automatic Test Equipment (ATE)
- Some parameters are assured by correlation to parameters tested on ATE
- Some parameters are checked manually using specialist test equipment (STE)
- Some parameters are assured by device design and the technology platform used
- Some parameters are assured by regular production process monitoring
- Some parameters are assured by regular reliability test monitoring

3. Parameters tested 100% by ATE

Certain parameters are 100% tested by ATE. All such parameters are tested repeatedly and with insets against the published datasheet limits to ensure a very high level of assurance for the values published.

3.1 V_{DRM}, V_{RRM}, I_D and I_R

Typically, these parameters are 100% tested for each individual die on the manufactured silicon wafers. V_{DRM} is tested to a minimum specification limit of 630V for a 600V series product, approximately a 5% "inset" or uplift on the voltage specification. Similarly, I_D is tested to the datasheet specification with the same higher applied voltage. In cases were the wafers have a very large number of dice and would require "lengthy" test time, a sample test of 100 dice per wafer is performed.

After assembly of the individual dice, the devices are 100% V_{DRM} tested to a minimum specification of 620V, approximately a 3.3% "inset" or uplift on the voltage specification of 600V. I_D is 100% tested to the datasheet specification for V_{DRM}.

Finally, an "Acceptance Test", "ACC" test is completed at the rated voltage datasheet specification for the parameters. This can be 100% testing in some cases or sample testing – e.g. 1250 devices from a 60-70k batch.

The reason for these "insets" or uplifts on the testing voltage specification is to protect against small calibration errors in test equipment and ensure integrity of the data value given in the datasheet.

3.2 I_{GT}

I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		2	-	50	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		2	-	50	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		2	-	50	mA

Maximum gate trigger current $I_{GT\,(max)}$ is a triac's or SCR's triggering need or requirement. The triggering circuit must apply at least this value of gate current to guarantee triggering the triac. If a minimum value is given in the datasheet, this indicates that current below that level – e.g. electrical noise will not trigger the SCR or triac.

It is important to understand these values are stated for 25 °C. I_{GT} increases as junction temperature decreases and so in order to guarantee reliable triggering of the triac or SCR, the designer needs set the gate drive current for the lowest operating temperature for the application. The minimum recommended gate pulse width for reliable triggering is 10µs.

Typically, this parameter is also 100% tested for each individual die on the manufactured silicon wafers with an "inset". In the example above, the testing would be to a 38.5mA limit. After assembly, the devices are 100% tested to within 3% for the gate current specification with a 48.5mA limit. A final "outgoing inspection test" is completed to the datasheet specification limit of 50mA. Similar appropriate insets are applied for any minimum limits also.

3.3 V_T

V_T	on-state voltage	I_T = 15 A; T_j = 25 °C; Fig. 10		-	1.3	1.6	V

V_T is the on-state voltage at 25 °C for a specified load current condition. This is the maximum instantaneous on-state voltage, measured under pulse conditions to avoid excessive power dissipation.

High current testing on wafers cannot be done accurately so although for low currents this parameter is 100% tested, for higher current devices the wafers are sample tested using 1250 devices from a batch of 60-70K devices. All assembled product is 100% tested after assembly.

4. Parameters correlated to those tested 100% by ATE

4.1 V_{GT}, I_H, I_L

These are parameters which sometimes cannot be 100% tested in the production process but are protected by correlation with those parameters that can be tested.

The "physics" governing the behaviour of triacs is such that there is a very good correlation for these "sensitivity related" parameters with I_{GT}.

The I_{GT} parameter is 100% ATE tested as described previously but it is understood that "correlation" between two parameters will always be subject to some spread in values and can vary a little in the volume production environment. Consequently, the maximum limits of such parameters in data are set such that there is a

significant safety margin. This means that the maximum limit for the I_{GT} testing will protect the data maximum limits on V_{GT}, I_H and I_L with plenty of "headroom".

At wafer stage these parameters are 100% tested whilst in other situations where numbers of dice may be very large the devices are sample tested using 1250 devices from a batch of 60-70K devices. All assembled product is 100% tested.

5. Parameters checked manually with specialist test equipment

5.1 dV_D/dt, dV_{com}/dt, dI_{com}/dt

The parameters related to "false trigger immunity" are dynamic parameters and these also have their values in data protected by correlation to other sensitivity related parameters such as I_{GT} which are 100% ATE tested. Although these dynamic parameters cannot be 100% tested on ATE, specialist manual or semi-automatic test methods are used for checking individual assembled devices to confirm the published data limits.

These false trigger immunity related parameters of off-state dV_D/dt and commutation parameters dV_{com}/dt and dI_{com}/dt are protected by correlation against a minimum limit on I_{GT} (or a minimum limit of an "I_{GT} derived parameter through some calculation formula"). This I_{GT} minimum limit is 100% tested. The limit is set in data to ensure there is plenty of "headroom" or safety margin where correlation is used.

The minimum, typical and maximum values for each parameter are based on measurements of deliberately large spread trials to produce devices at WeEn's process-window limits. From these measurements, a value measured as a "minimum" represents what the worst-case device in the production-spread would be. However, the guaranteed minimum as shown in the datasheet is set at a value a little lower than this measured worst-case performance. This gives designers a further extra safety margin. Similarly, the values measured as "maximum" are a measure of the best-case performance in the production-spread of devices. They do not represent guaranteed maximum values. A guaranteed maximum is not of use to designers in a circuit application because the guaranteed minimum is the important parameter for "false trigger immunity". It is possible however to make a rough inference that if the measured parameters are a normal gaussian-shaped distribution (this is normally the case for production-spreads), then the maximum value should roughly be higher than the typical value by as much as the minimum value is below the typical.

6. Parameters and ratings protected by design and technology

6.1 $T_{j\,(max)}$, $T_{stg\,(max)}$, I_{TSM}, dI_T/dt, P_{GM}, $P_{G(AV)}$, I_{GM}, R_{th}

Certain parameters and ratings are inherent to the wafer manufacturing and package assembly technology. These are therefore protected by design.

The temperature ratings have been tested extensively through zero hour and reliability testing as well as also regularly checked with WeEn's routine monitoring life testing program.

Other ratings such as I_{TSM}, turn-on dI_T/dt, gate ratings and thermal resistance, R_{th} are specified in accordance with silicon chip design (MT1 or Anode, MT2 or Cathode and gate structure) as well as assembly methods for the finished device. The rules for setting limits on these parameters apply across a whole range of products within WeEn's triac technology family.

7. Parameters assured by constant production process monitoring

Certain tests are carried out to monitor the production process and certain parameters are tested which are not included in the published datasheet. This assures the reliability and integrity of the production and assembly processes. These tests are done regularly as sample tests or 100% tests.

For example, a parameter called “deltaVT” is used to monitor and indicate die attach quality after assembly.

In another example, Qs is a measure of stored charge for SCRs and is a wafer tested to a *minimum* limit (whether 100% ATE or manual). This protects against wafers having low Qs due to incoming wafer quality or process issues (such as contamination). In this example, the minimum Qs limit is to protect *other parameters* in the final product, such as ITSM in SCRs.

Ultrafast diodes with a maximum Qs/trr specification in the datasheet would normally have a 100% maximum Qs or trr test to protect this parameter. In some cases, this is done by a “minimum V_F” test. At the wafer test stage this is usually done manually on a few points per wafer to “protect assembly yields”, by ensuring wafers delivered for assembly are not wrongly processed.

8. Parameters assured by regular reliability test monitoring

Routine reliability test monitoring is performed every 3 months. A sample selection of devices with similar structure are chosen for these tests. Each technology platform with every package type is included in the choice. Six to seven reliability tests are carried out for each selected product type using 80 devices with control samples.

9. Product reliability robustness – a pictorial view

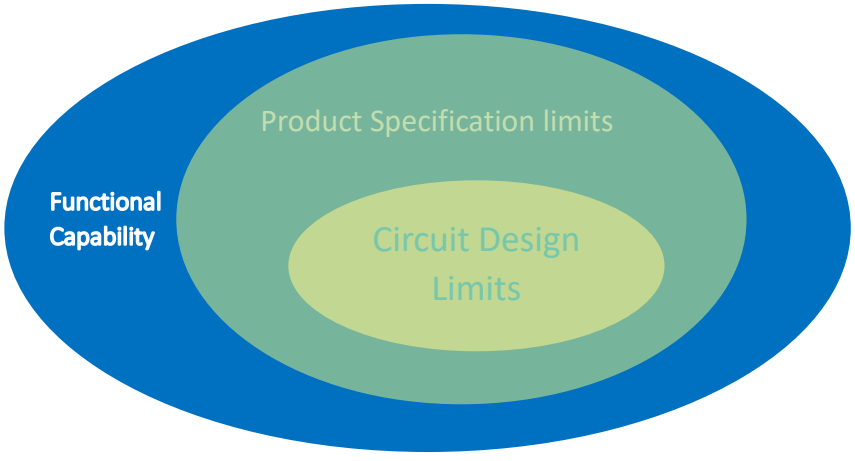

Fig 1. Representation of data integrity and relationship with capability, data limits and circuit design limits

Revision history

Rev	Date	Description
v.01	20191106	initial version

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