ACTT4S-800ETN

AC Thyristor Triac power switch

Rev.01 - 23 July 2025 Product data sheet

1. General description

AC Thyristor Triac power switch in a DPAK surface mountable plastic package with self-protective clamping capabilities against low and high energy transients. This "series ETN" triac will commutate the full RMS current at the maximum rated junction temperature ($T_{j(max)}$ = 150 °C) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

4. Quick reference data

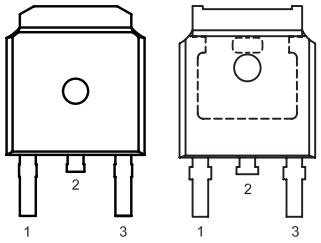
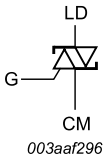
Table 1. Quick reference data

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DRM}	repetitive peak off-state voltage			800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 131$ °C; Fig. 1; Fig. 2; Fig. 3		4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		40	A
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms		44	A
T_j	operating junction temperature			-40 to 150	°C

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; LD+ G+; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 0.1 A; LD+ G-; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 0.1 A; LD- G-; T_j = 25 °C; Fig. 8		-	-	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	30	mA
V_T	on-state voltage	I_T = 5 A; T_j = 25 °C; Fig. 11		-	-	1.6	V
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; $R_{G(T1)}$ = 220 Ω		2000	-	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common		
2	LD	load		
3	G	gate		
mb	LD	mounting base; load		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
ACTT4S-800ETN	TO252	ACTT4S-800ETNJ	Reel	2500	TO252N	04-Nov-2016
					TO252Q	05-Mar-2025

7. Marking

Table 4. Marking codes

Type number	Marking codes	
	Assembly factory: N	Assembly factory: Q
ACTT4S-800ETN	ACTT4S 800ETN PJNxxxx xx	ACTT4S 800ETN PJQxxxx xx

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DRM}	repetitive peak off-state voltage			800	V
V_{RRM}	repetitive peak reverse voltage			800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 131$ °C; Fig. 1; Fig. 2; Fig. 3		4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig 4; Fig 5		40	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		44	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		8	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 20$ mA		100	A/µs
I_{GM}	peak gate current	$t_p = 20$ µs		4	A
P_{GM}	peak gate power			10	W
$P_{G(AV)}$	average gate power	over any 20 ms period		0.5	W
T_{stg}	storage temperature			-40 to 150	°C
T_j	operating junction temperature			-40 to 150	°C
V_{PP}	peak pulse voltage	$T_j = 25$ °C; non-repetitive off-state; Fig. 6		2	kV

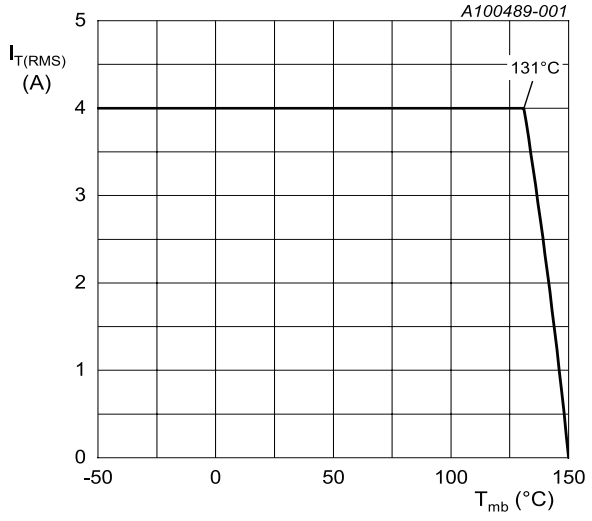
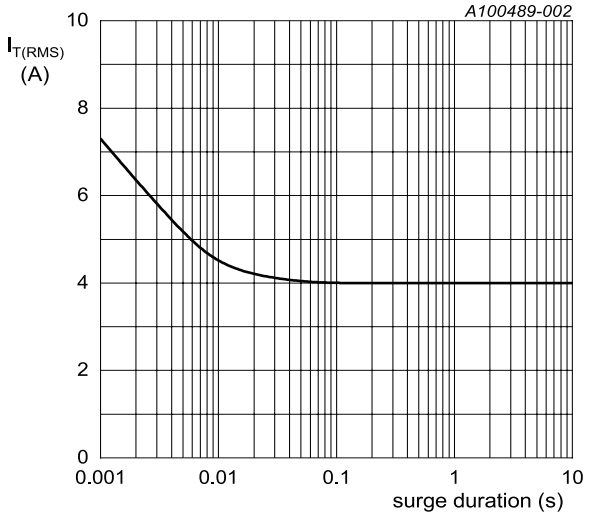
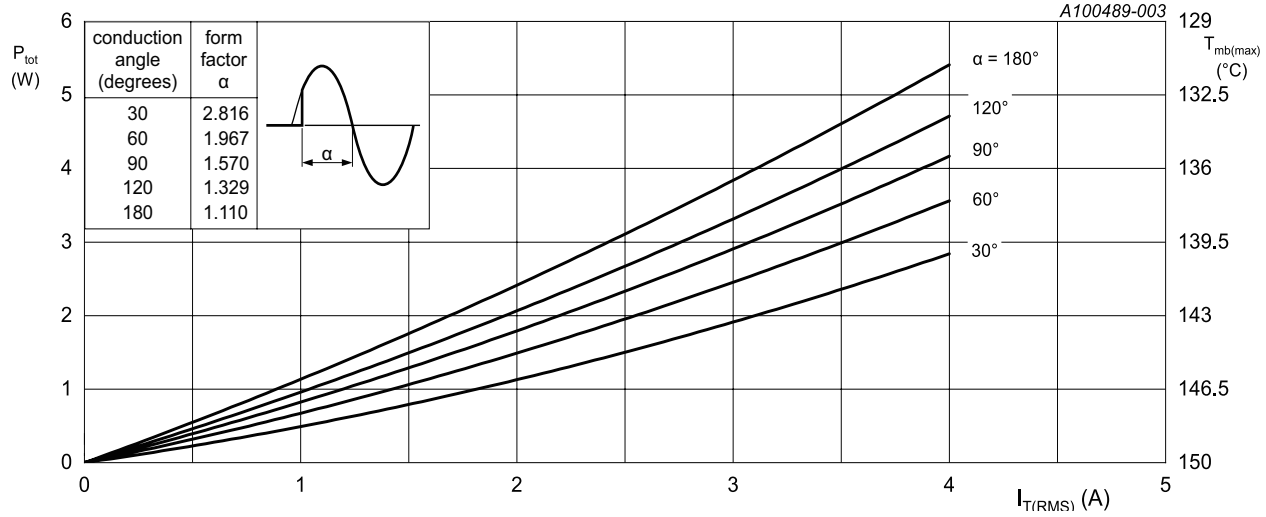


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz; $T_{mb} = 131$ °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values

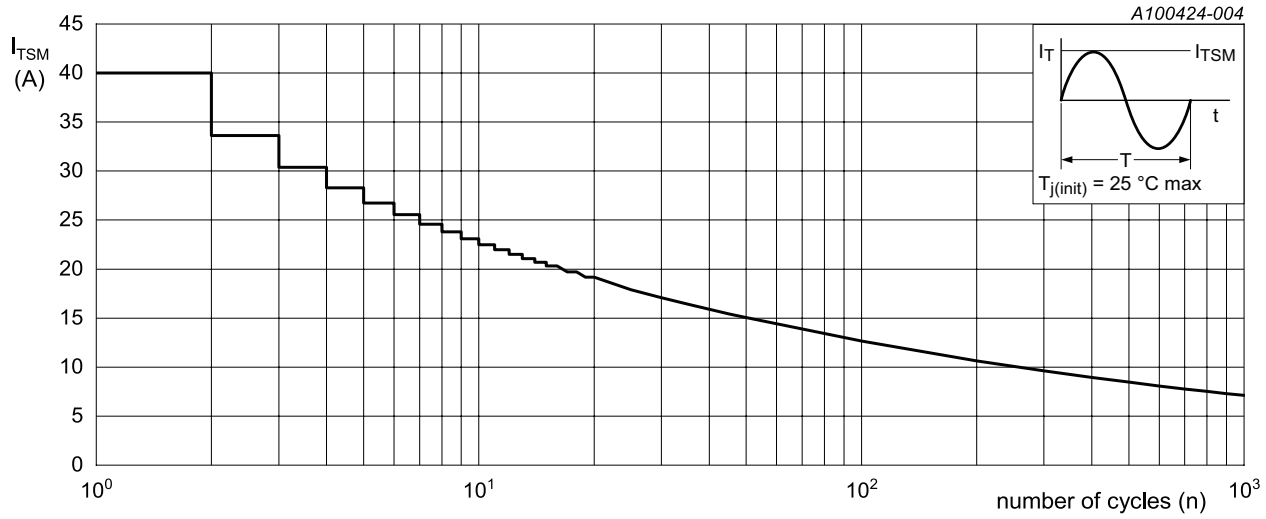


conduction angle (degrees)	form factor α
30	2.816
60	1.967
90	1.570
120	1.329
180	1.110

α = conduction angle

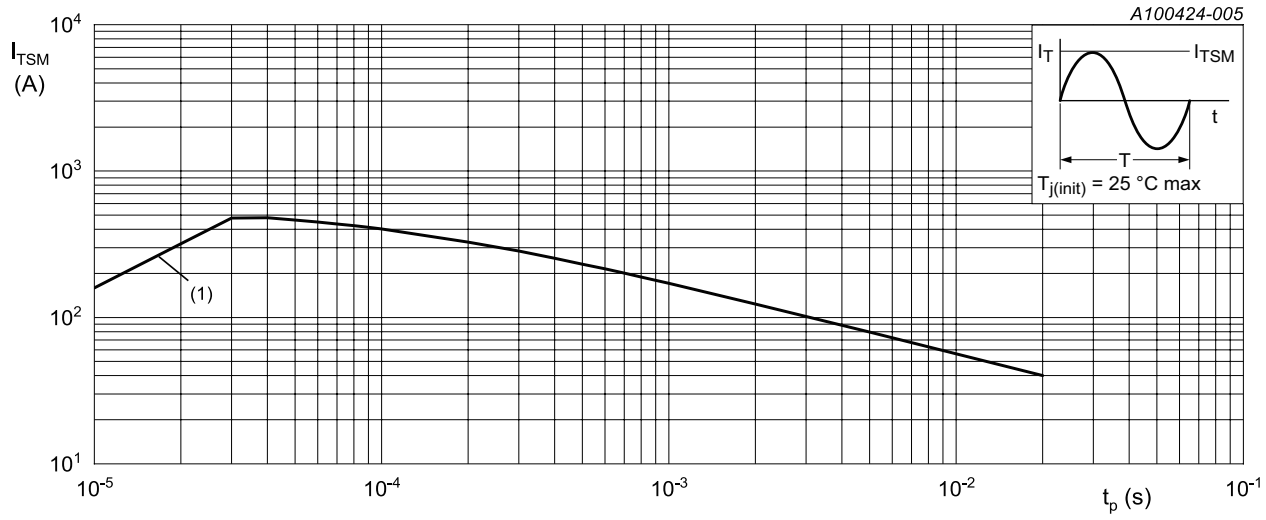
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

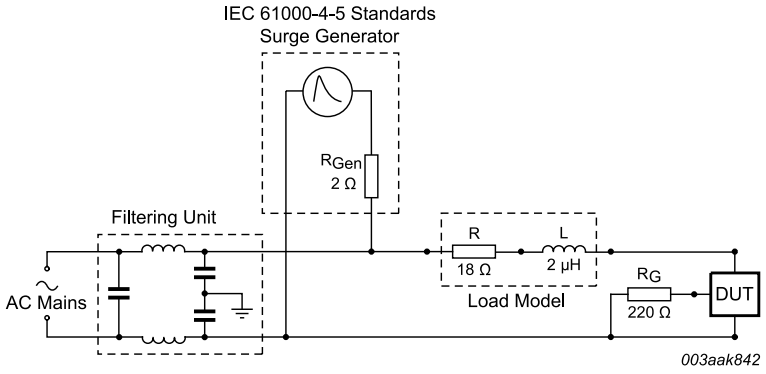


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 7		-	-	3.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; printed circuit board (FR4) mounted		-	50	-	K/W

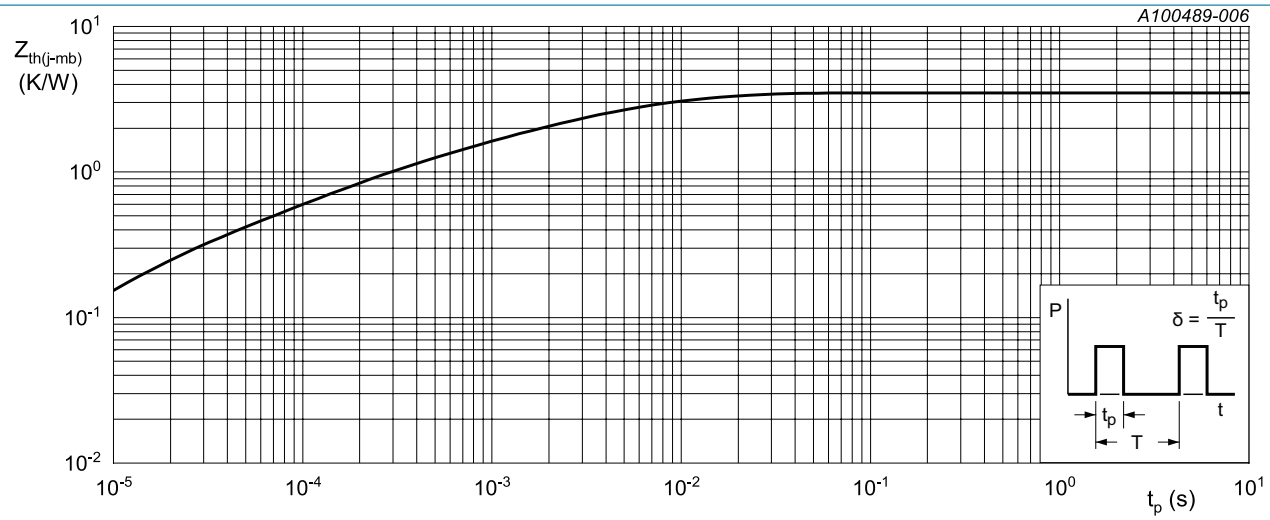
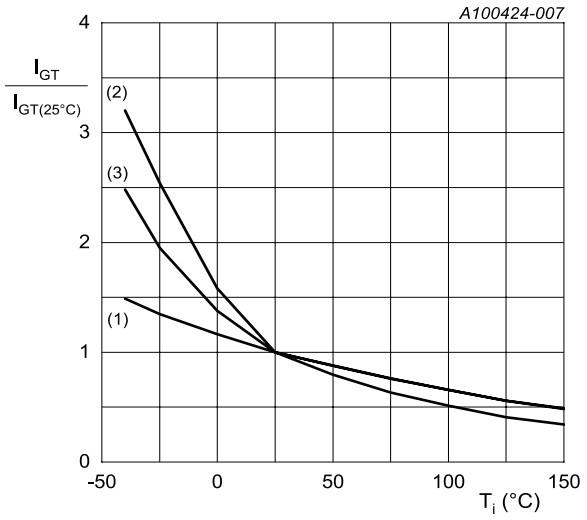


Fig. 7. Transient thermal impedance from junction to mounting base as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; LD+ G+; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 0.1 A; LD+ G-; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 0.1 A; LD- G-; T_j = 25 °C; Fig. 8		-	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; LD+ G+; T_j = 25 °C; Fig. 9		-	-	40	mA
		V_D = 12 V; I_G = 0.1 A; LD+ G-; T_j = 25 °C; Fig. 9		-	-	50	mA
		V_D = 12 V; I_G = 0.1 A; LD- G-; T_j = 25 °C; Fig. 9		-	-	40	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	30	mA
V_T	on-state voltage	I_T = 5 A; T_j = 25 °C; Fig. 11		-	-	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 12		-	-	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 150 °C; Fig. 12		0.3	-	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 150 °C		-	-	2	mA
I_R	reverse current	V_R = 800 V; T_j = 25 °C		-	-	10	µA
		V_R = 800 V; T_j = 150 °C		-	-	2	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; $R_{G(T1)}$ = 220 Ω		2000	-	-	V/µs



(1) LD+ G+
(2) LD+ G-
(3) LD- G-

Fig. 8. Normalized gate trigger current as a function of junction temperature

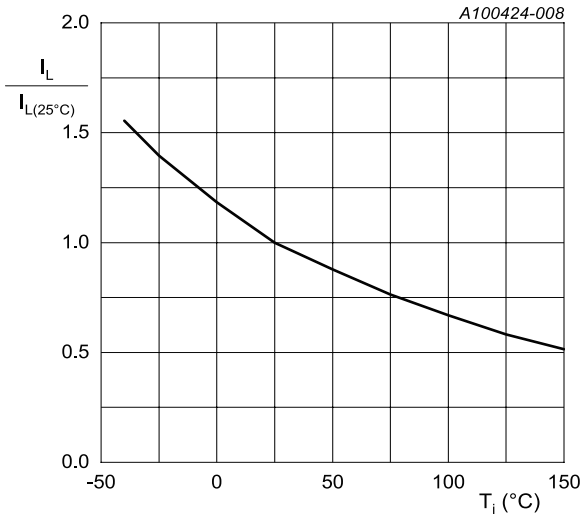


Fig. 9. Normalized latching current as a function of junction temperature

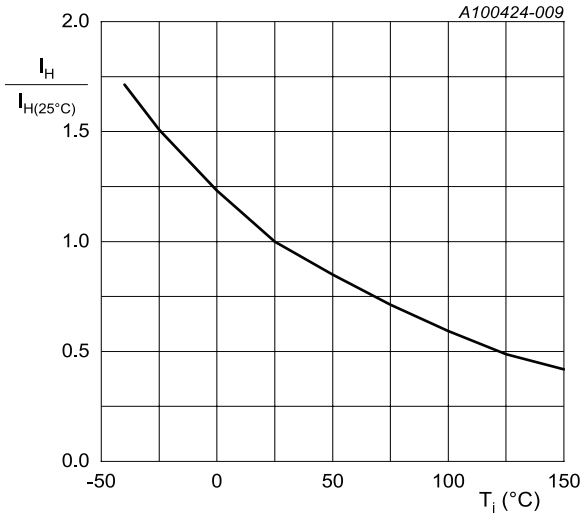
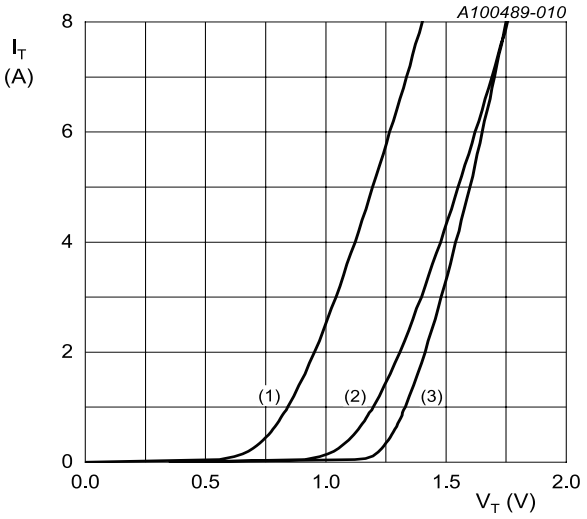


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.178 V; R_s = 0.0730 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

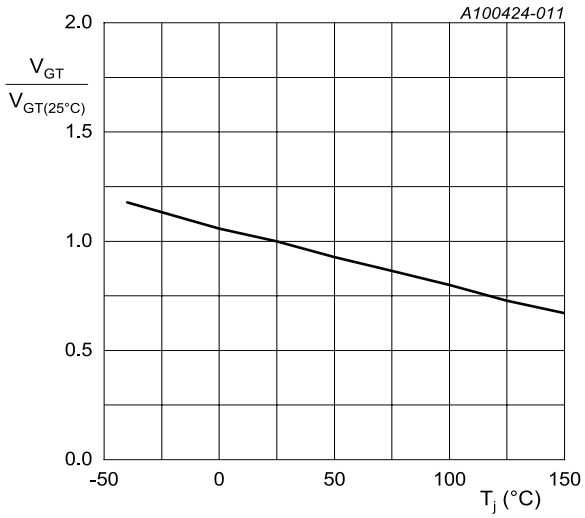
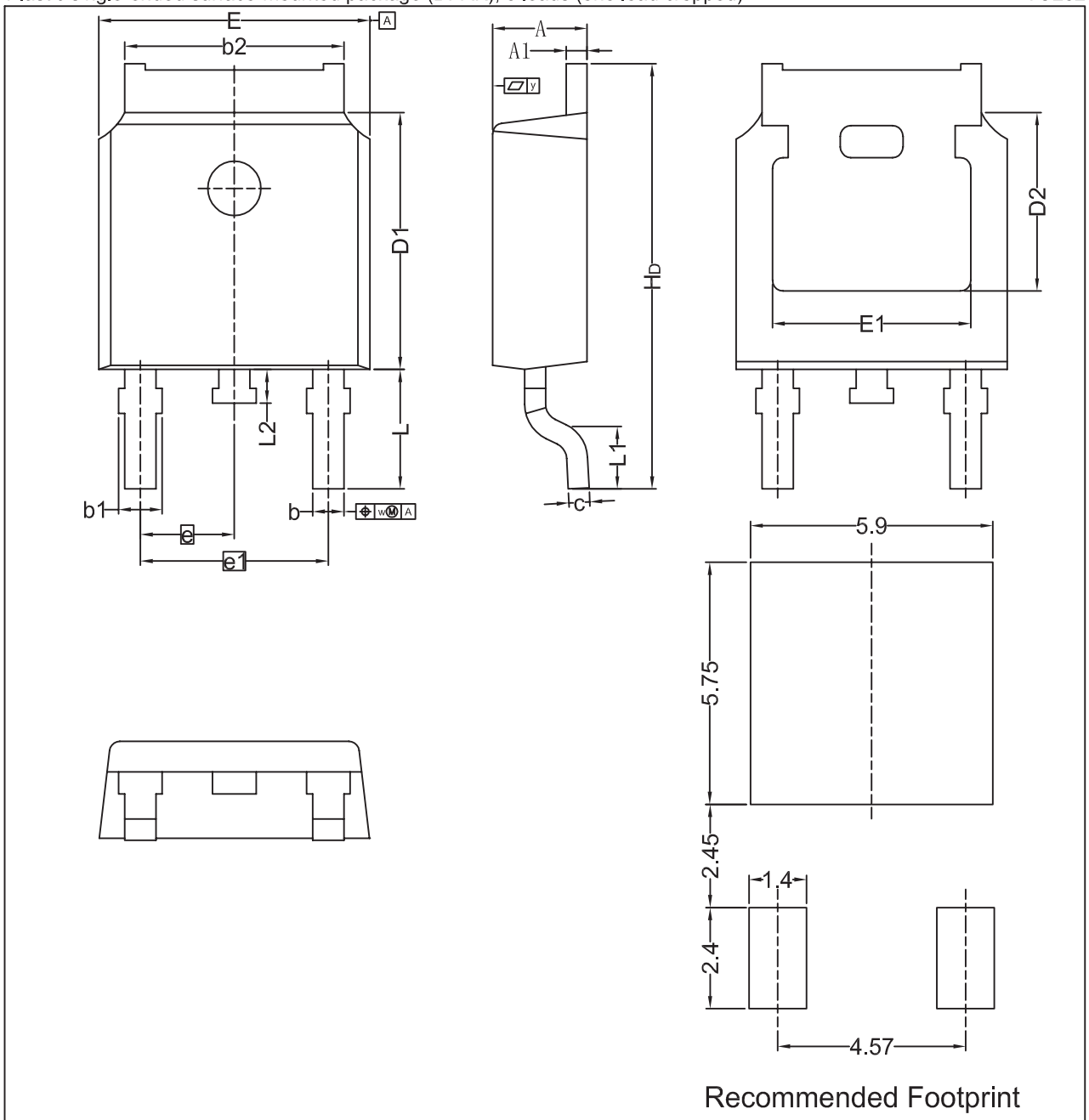


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Assembly factory: N

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) TO252

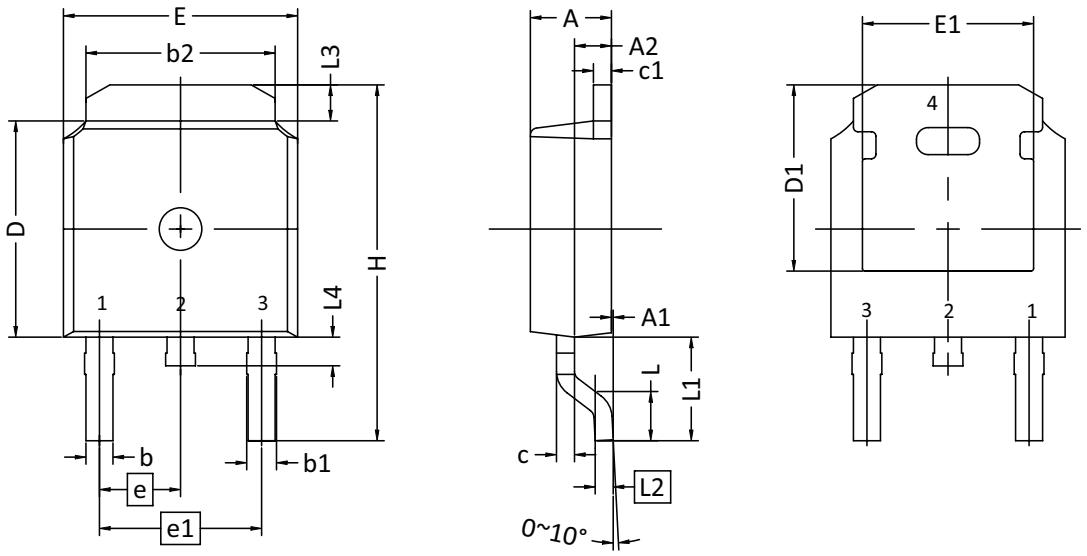


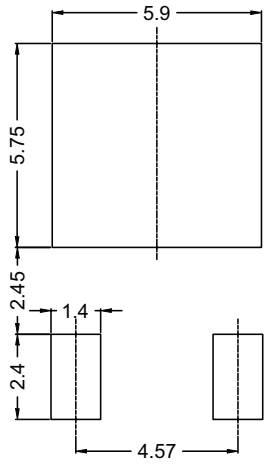
Recommended Footprint

Unit	A	A1	b	b1	b2	c	D1	D2	E	E1	e	e1	H_D	L	L1	L2	w	y
min	2.22	0.46	0.71	0.72	5.00	0.20	5.98	4.00	6.47	4.45	2.285	4.57	9.60	2.90 (Ref.)	0.50	0.50	0.20	
mm nom																		
max	2.38	0.93	0.89	1.10	5.46	0.56	6.22	---	6.73	---			10.40		---	0.90		0.20

Assembly factory: Q

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) TO252





Recommended Footprint

SYMBOLS	DIMENSION IN MM		
	MIN	NOM	MAX
A	2.184	2.286	2.400
A1	0.000	---	0.200
A2	0.889	1.041	1.170
b	0.635	0.762	0.889
b1	0.680	0.840	1.143
b2	4.953	5.340	5.500
c	0.450	0.508	0.610
c1	0.450	0.508	0.630
D	5.969	6.096	6.223
D1	5.210	5.249	5.380
E	6.350	6.604	6.800
E1	4.318	4.826	4.920
e	2.286BSC		
e1	4.572BSC		
H	9.398	10.033	10.500
L	1.270	1.520	2.032
L1	2.921REF		
L2	0.408	0.508	0.608
L3	0.889	1.016	1.270
L4	0.600	---	1.016

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

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Date of release: 23 July 2025