

1. General description

WeEn Gen-2 Silicon Carbide MOSFET in a TSPAK plastic package, featured with top side cooling structure, designed for high frequency, high efficiency systems.



2. Features and benefits

- Top side cooling structure
- Kelvin source configuration
- Low specific on-resistance
- Optimized dynamic performance
- Robust gate design
- 0V turn-off V_{GS} for simple gate driving
- 100% UIS Tested
- Easy to parallel
- RoHS compliant



3. Applications

- PC/server/telecom power supplies
- UPS & Energy storage system
- Battery formation instrument
- PV MPPT and inverters
- EV Chargers
- Motor Drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Notes	Values			Unit
Absolute maximum rating							
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		650			V
I_D	drain current	$V_{GS} = 18\text{ V}; T_{mb} = 25\text{ °C}$		152			A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}, T_j = 175\text{ °C}$		500			W
T_j	junction temperature			-55 to 175			°C
Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 15\text{ V}; I_D = 55\text{ A}; T_j = 25\text{ °C}$		-	19	-	mΩ
		$V_{GS} = 18\text{ V}; I_D = 55\text{ A}; T_j = 25\text{ °C}$		-	15	20	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 55\text{ A}; V_{DS} = 400\text{ V}; V_{GS} = -4\text{ V}/18\text{ V}; T_j = 25\text{ °C}$		-	155	-	nC
Q_{GD}	gate-drain charge			-	18.2	-	nC
Source-drain diode							
Q_r	recovered charge	$I_{SD} = 55\text{ A}; di/dt = 500\text{ A}/\mu\text{s}; V_{DS} = 400\text{ V}; T_j = 25\text{ °C}$		-	170	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	SS	source sense		
3-7	S	source		
8-9 mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
WNSC2M19065TB	TSPAK	WNSC2M19065TB6J	Reel	600	TSPAKH	06-Dec-2024

7. Marking

Table 4. Marking codes

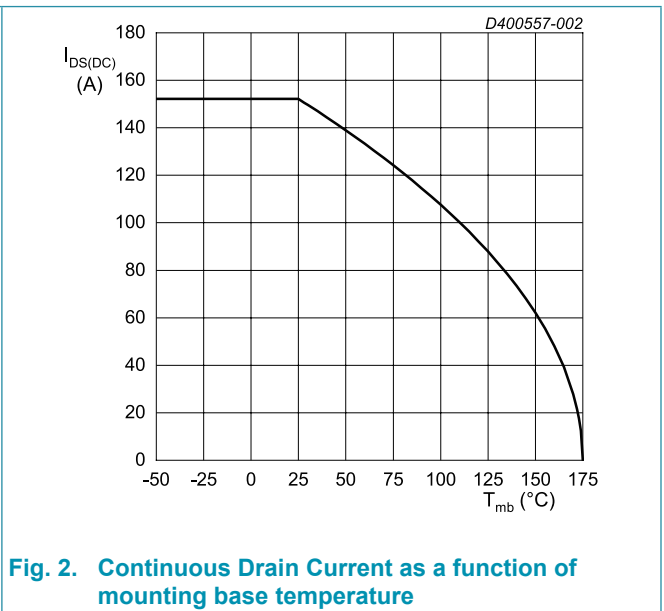
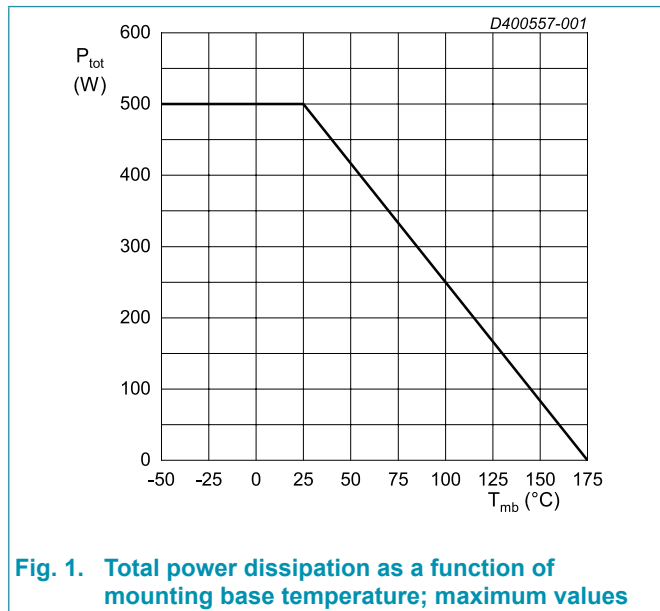
Type number	Marking codes
WNSC2M19065TB	WNSC2M 19065TB

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		650	V
$V_{GS,max}$	gate-source voltage	Absolute maximum values		-10 to 22	V
$V_{GS,op}$	gate-source voltage	Recommended operational values		-4 to 18	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}, T_j = 175\text{ °C}$		500	W
I_D	drain current	$V_{GS} = 18\text{ V}; T_{mb} = 25\text{ °C}$		152	A
		$V_{GS} = 18\text{ V}; T_{mb} = 100\text{ °C}$		108	A
I_{DM}	peak drain current	pulse width t_p limited by T_{jmax}	Fig.17	304	A
I_S	continuous diode current	$V_{GS} = -4\text{ V}; T_{mb} = 25\text{ °C}$		92	A
I_{SM}	pulse diode current	$V_{GS} = -4\text{ V};$ pulse width t_p limited by T_{jmax}		304	A
E_{as}	single pulse drain-to-source avalanche	$I_{AS} = 28.6\text{ A}; L = 1\text{ mH}; V_{DD} = 100\text{ V}; T_j = 25\text{ °C}$		408	mJ
T_{stg}	storage temperature			-55 to 175	°C
T_j	junction temperature			-55 to 175	°C
$T_{sld(M)}$	peak soldering temperature			260	°C



9. Thermal & Mechanical characteristics

Table 6. Thermal & Mechanical characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	0.3	-	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	40	-	K/W

Note: Device is ESD sensitive. Handling precautions are recommended.

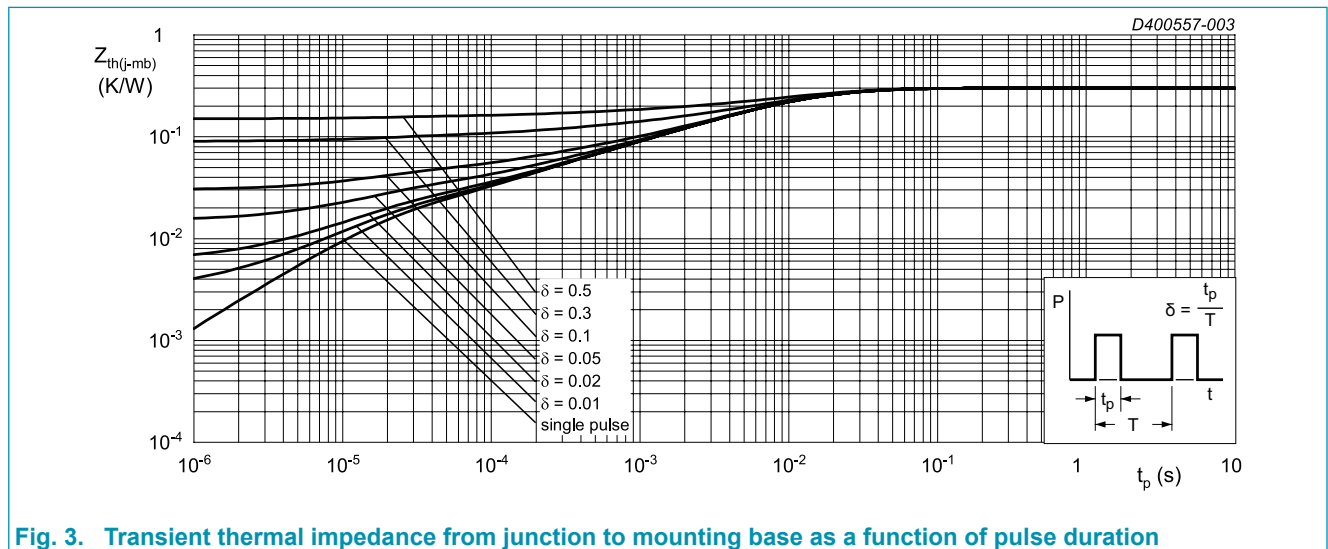
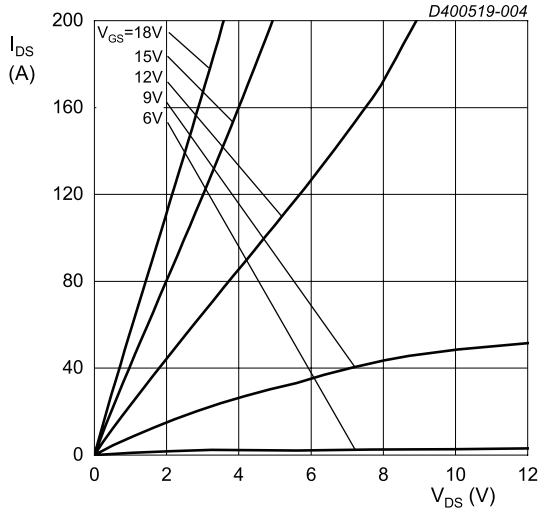


Fig. 3. Transient thermal impedance from junction to mounting base as a function of pulse duration

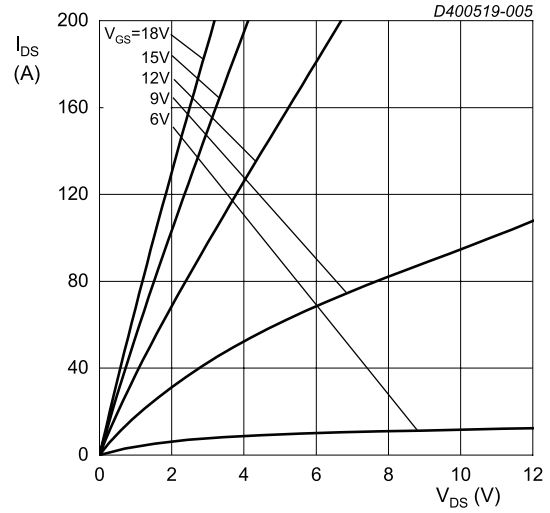
10. Characteristics

Table 7. Characteristics

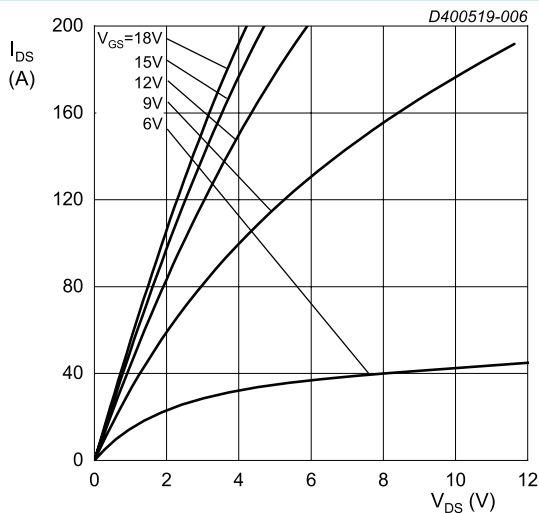
Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 100 \mu A; V_{GS} = 0 V; T_J = 25 \text{ }^\circ C$		650	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 14 \text{ mA}; V_{DS} = V_{GS}; T_J = 25 \text{ }^\circ C$		1.9	2.6	3.5	V
		$I_D = 14 \text{ mA}; V_{DS} = V_{GS}; T_J = 175 \text{ }^\circ C$		-	1.9	-	V
I_{DSS}	drain leakage current	$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ C$		-	0.1	50	μA
		$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 175 \text{ }^\circ C$		-	5	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 22 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ C$		-	5	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ C$		-	5	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 15 \text{ V}; I_D = 55 \text{ A}; T_J = 25 \text{ }^\circ C$		-	19	-	m Ω
		$V_{GS} = 18 \text{ V}; I_D = 55 \text{ A}; T_J = 25 \text{ }^\circ C$		-	15	20	m Ω
		$V_{GS} = 18 \text{ V}; I_D = 55 \text{ A}; T_J = 175 \text{ }^\circ C$		-	18	-	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_J = 25 \text{ }^\circ C$		-	1.05	-	Ω
g_{fs}	transconductance	$V_{DS} = 20 \text{ V}; I_D = 55 \text{ A}; T_J = 25 \text{ }^\circ C$		-	42	-	S
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 55 \text{ A}; V_{DS} = 400 \text{ V}; V_{GS} = -4 \text{ V}/18 \text{ V}; T_J = 25 \text{ }^\circ C$		-	155	-	nC
Q_{GS}	gate-source charge			-	61	-	nC
Q_{GD}	gate-drain charge			-	18.2	-	nC
C_{iss}	input capacitance	$V_{DS} = 400 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_J = 25 \text{ }^\circ C$		-	3730	-	pF
C_{oss}	output capacitance			-	307	-	pF
C_{rss}	reverse transfer capacitance			-	17	-	pF
E_{oss}	Coss stored energy			-	24.6	-	μJ
$t_{d(on)}$	turn-on delay time	$V_{DS} = 400 \text{ V}; V_{GS} = -4 \text{ V}/18 \text{ V}; R_{G(ext)} = 5.1 \text{ } \Omega; I_D = 27.5 \text{ A}; L = 100 \text{ } \mu H; T_J = 25 \text{ }^\circ C$		-	24	-	ns
t_r	rise time			-	24	-	ns
$t_{d(off)}$	turn-off delay time			-	58	-	ns
t_f	fall time			-	15	-	ns
E_{on}	turn-on energy (Body Diode FWD)			Fig.19	-	130	-
E_{off}	turn-off energy (Body Diode FWD)		Fig.19	-	32	-	μJ
Source-drain diode							
V_{SD}	source-drain voltage	$V_{GS} = 0 \text{ V}; I_{SD} = 55 \text{ A}; T_J = 25 \text{ }^\circ C$		-	3.7	-	V
		$V_{GS} = -4 \text{ V}; I_{SD} = 55 \text{ A}; T_J = 25 \text{ }^\circ C$		-	4.2	-	V
		$V_{GS} = -4 \text{ V}; I_{SD} = 55 \text{ A}; T_J = 175 \text{ }^\circ C$		-	3.7	-	V
t_{rr}	reverse recovery time	$I_{SD} = 55 \text{ A}; di/dt = 500 \text{ A}/\mu s; V_{DS} = 400 \text{ V}; T_J = 25 \text{ }^\circ C$		-	41.2	-	ns
Q_r	recovered charge			-	170	-	nC
I_{rrm}	reverse recovery current			-	8.2	-	A



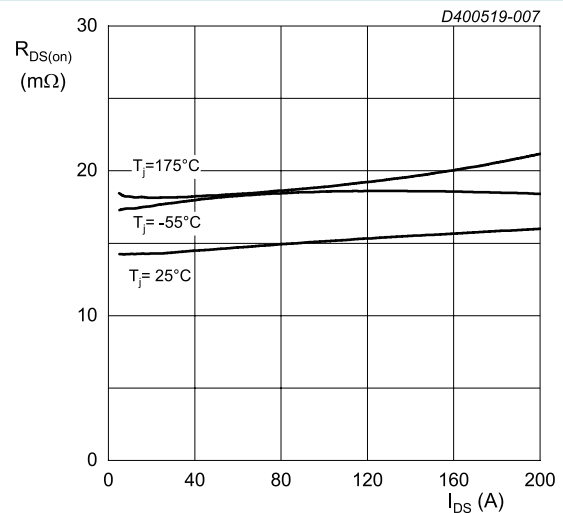
$T_j = -55\text{ }^\circ\text{C}; t_p < 200\text{ }\mu\text{s}$
Fig. 4. Output characteristics; drain current as a function of drain-source voltage; typical values



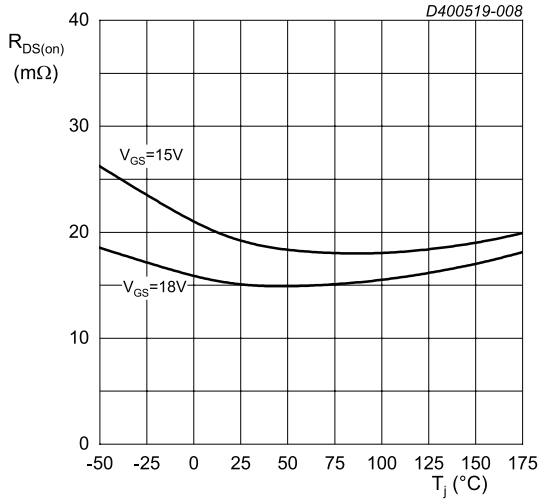
$T_j = 25\text{ }^\circ\text{C}; t_p < 200\text{ }\mu\text{s}$
Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values



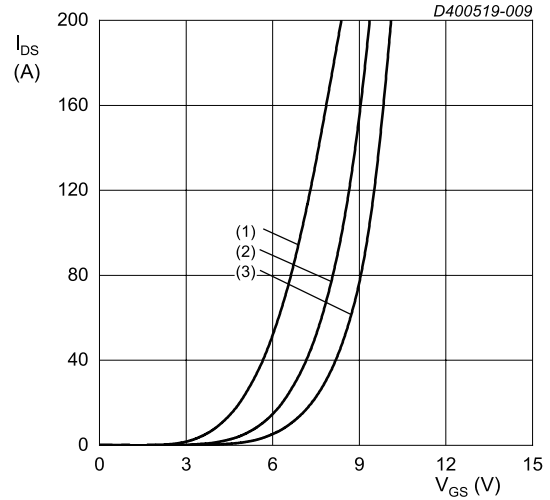
$T_j = 175\text{ }^\circ\text{C}; t_p < 200\text{ }\mu\text{s}$
Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



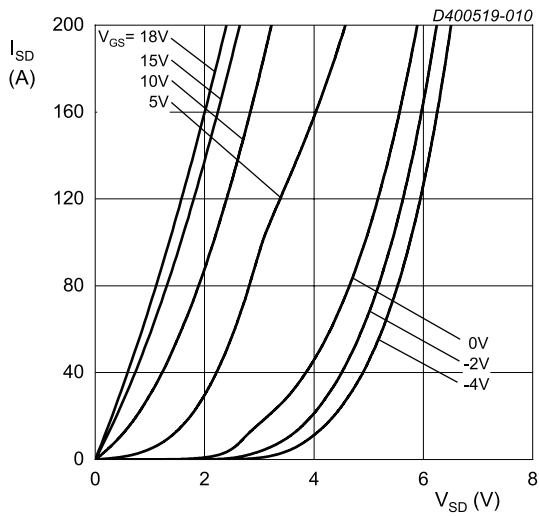
$V_{GS} = 18\text{ V}; t_p < 200\text{ }\mu\text{s}$
Fig. 7. Drain-source on-state resistance as a function of drain current; typical values



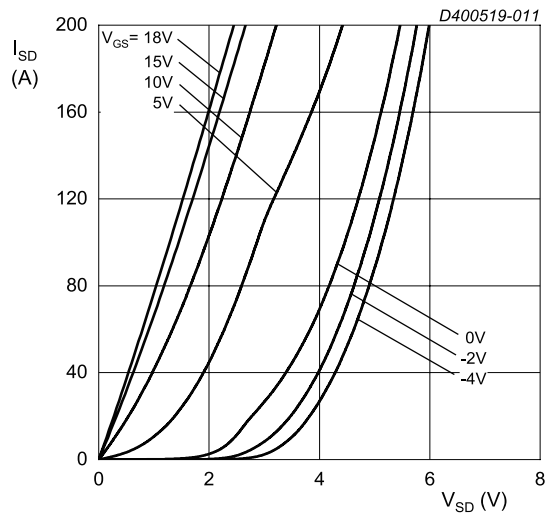
$I_{DS} = 55 A; t_p < 200 \mu s$
Fig. 8. Drain-source on-state resistance as a function of junction temperature



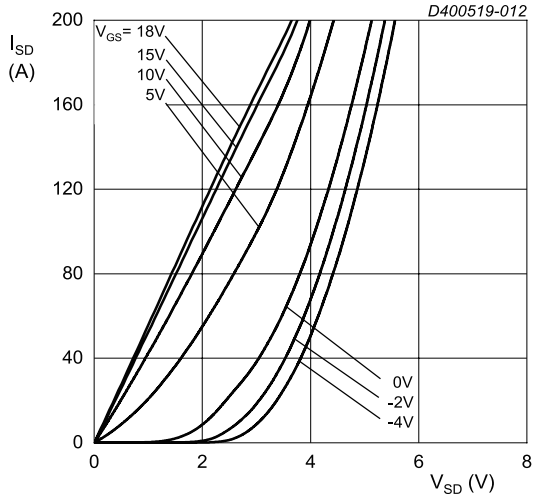
$V_{DS} = 20 V; t_p < 200 \mu s$
 (1) $T_j = 175^{\circ}C$
 (2) $T_j = 25^{\circ}C$
 (3) $T_j = -55^{\circ}C$
Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



$T_j = -55^{\circ}C; t_p < 200 \mu s$
Fig. 10. Body diode forward characteristics; typical values

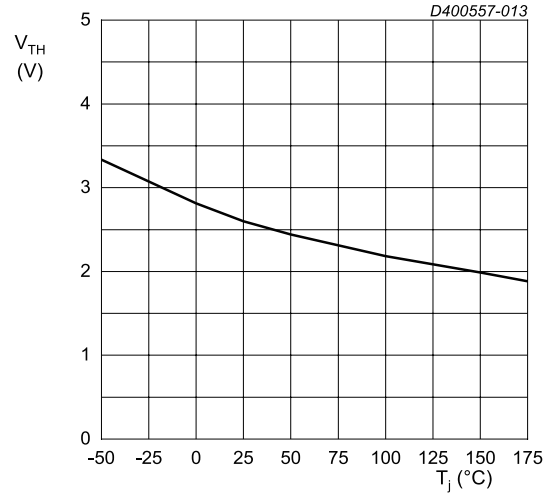


$T_j = 25^{\circ}C; t_p < 200 \mu s$
Fig. 11. Body diode forward characteristics; typical values



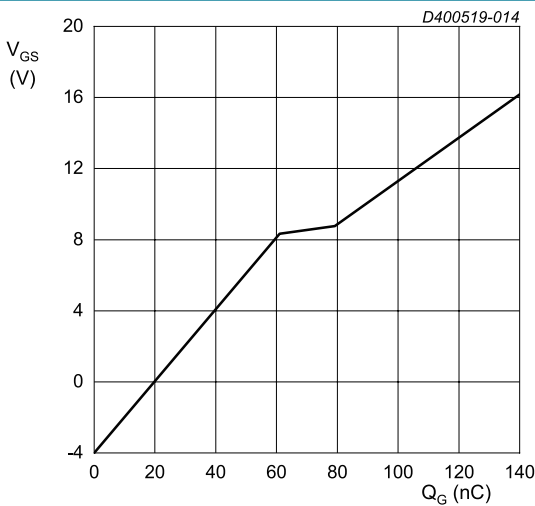
$T_j = 175\text{ }^\circ\text{C}$; $t_p < 200\text{ }\mu\text{s}$

Fig. 12. Body diode forward characteristics; typical values



$V_{DS} = V_{GS}$; $I_{DS} = 14\text{ mA}$

Fig. 13. Threshold voltage as a function of junction temperature



$I_{DS} = 55\text{ A}$; $I_{GS} = 0.1\text{ mA}$; $V_{DS} = 400\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

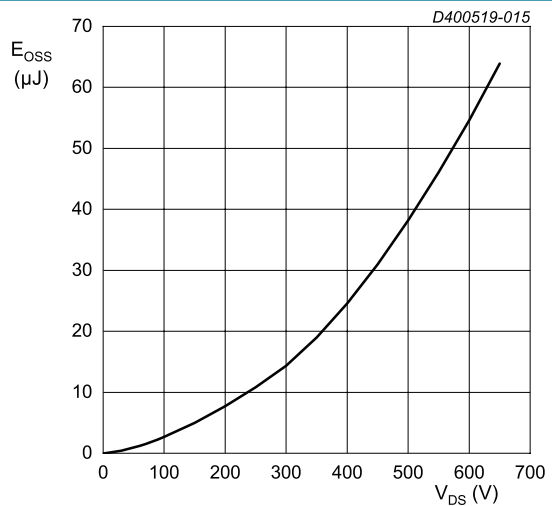
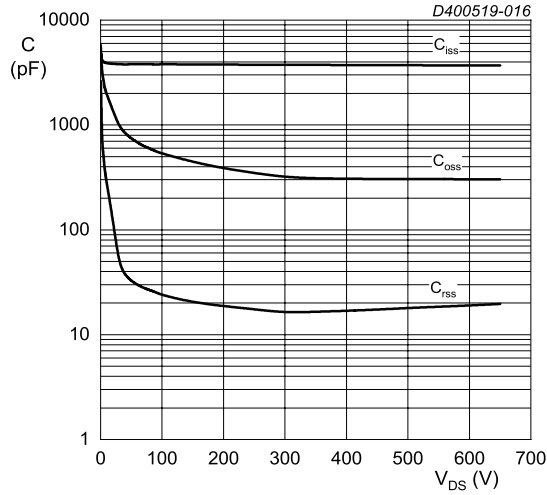
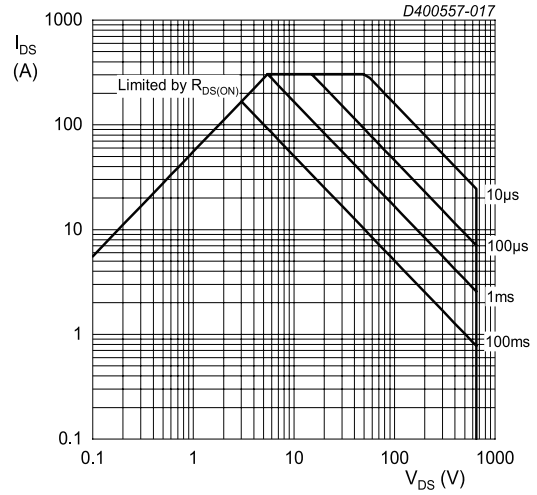


Fig. 15. Output capacitor stored energy as a function of drain-source voltage



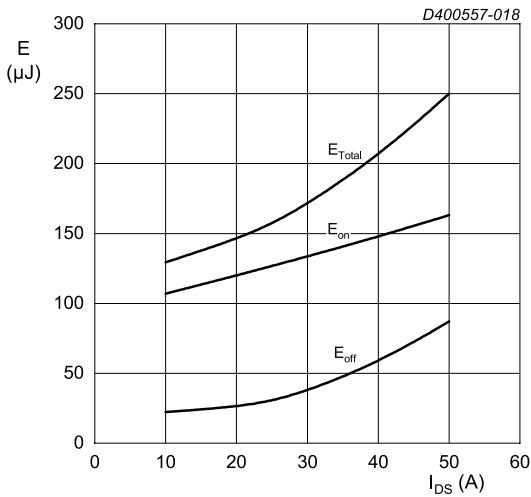
V_{DS} = 0 - 650 V
 T_j = 25 °C; V_{AC} = 25 mV; f = 1 MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



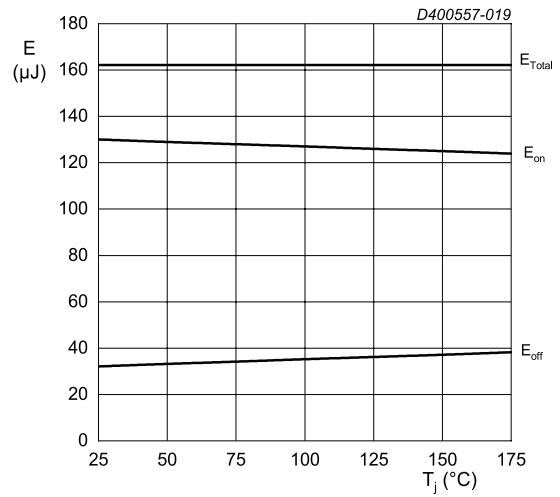
T_j = 25 °C; D = 0
 Parameter: t_p

Fig. 17. Forward bias safe operating area



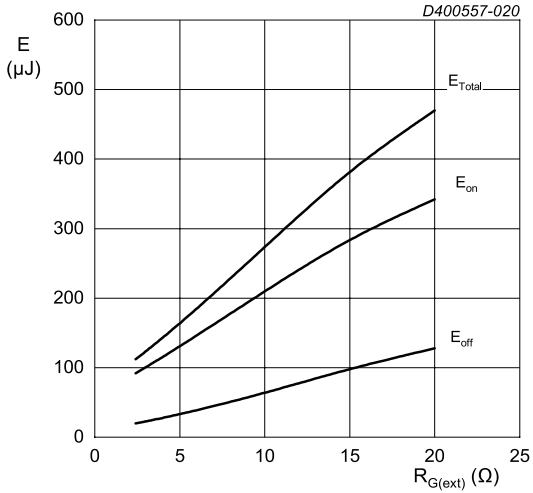
T_j = 25 °C; V_{DD} = 400 V; R_{G(ext)} = 5.1 Ω;
 V_{GS} = -4 V/18 V; L = 100 µH
 FWD = WNSC2M19065TB

Fig. 18. Clamped Inductive Switching Energy as a function of drain current



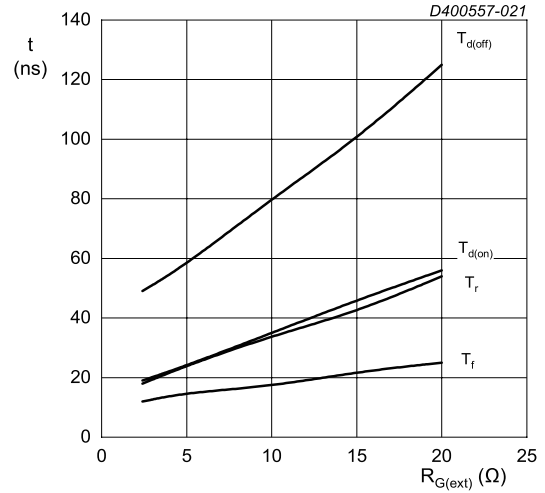
I_{DS} = 27.5 A; V_{DD} = 400 V; R_{G(ext)} = 5.1 Ω;
 V_{GS} = -4 V/18 V; L = 100 µH
 FWD = WNSC2M19065TB

Fig. 19. Clamped Inductive Switching Energy as a function of junction temperature



T_j = 25 °C; V_{DD} = 400 V; I_{DS} = 27.5 A; V_{GS} = -4 V/18 V
FWD = WNSC2M19065TB; L = 100 μH

Fig. 20. Clamped Inductive Switching Energy as a function of external gate resistance



T_j = 25 °C; V_{DD} = 400 V; I_{DS} = 27.5 A; V_{GS} = -4 V/18 V
FWD = WNSC2M19065TB; L = 100 μH

Fig. 21. Switching time as a function of external gate resistance

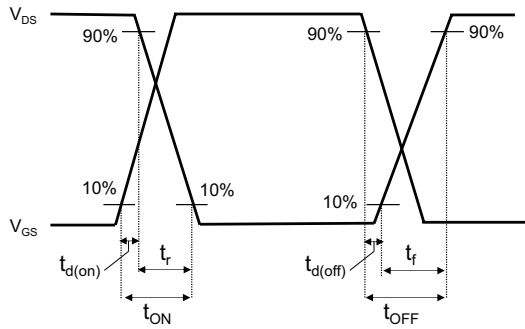
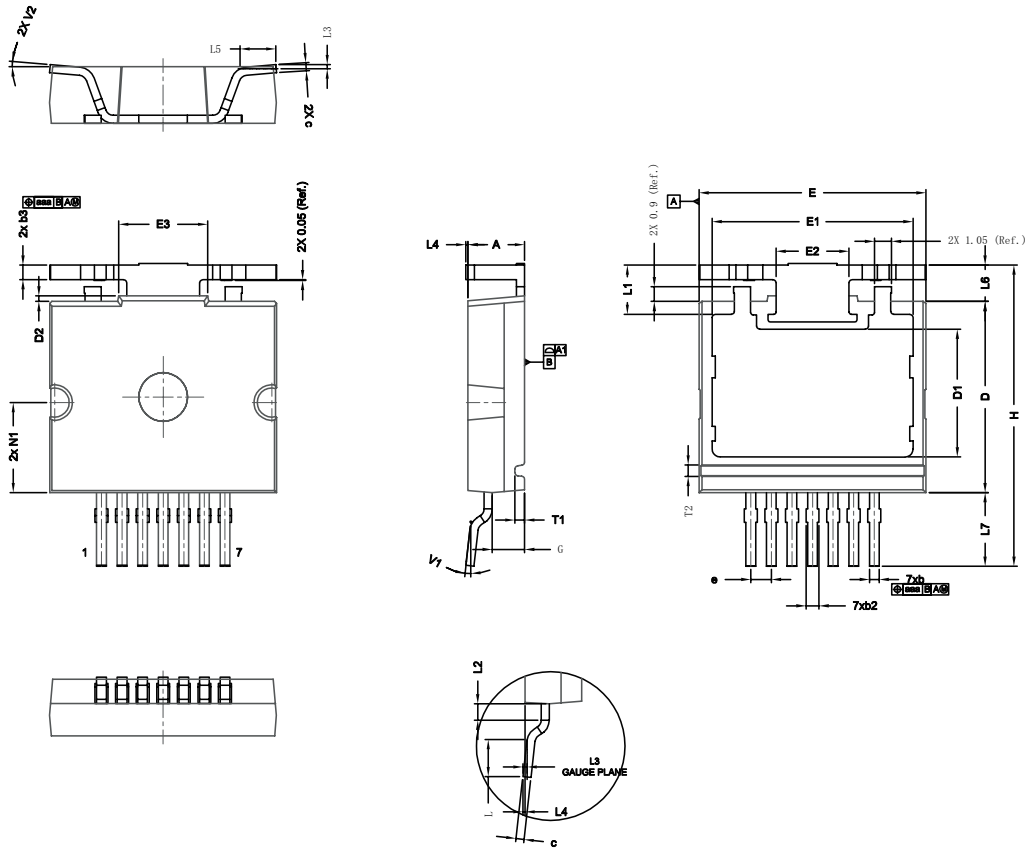
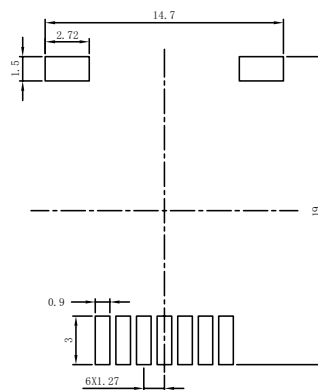


Fig. 22. Switching time definition

11. Package outline



SYMBOL	DIMENSIONS MILLIMETER			SYMBOL	DIMENSIONS MILLIMETER		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	3.40	3.50	3.60	H	18.00	18.58	19.00
A1	0.05			L	2.185	2.285	2.385
b	0.50	0.60	0.70	L1	3.04		
b2	0.70	0.80	0.90	L2	0.90	1.00	1.10
b3	0.80	0.90	0.98	L3	0.26		
c	0.40	0.50	0.60	L4	0.075	0.125	0.175
D	11.70	11.80	11.90	L5	2.10	2.20	2.30
D1	7.78	7.88	7.98	L6	2.14	2.24	2.34
D2	0.24	0.34	0.44	L7	4.44	4.54	4.64
E	13.90	14.00	14.10	N1	5.46	5.56	5.66
E1	12.30	12.40	12.50	T1	0.6(Ref)		
E2	4.45	4.50	4.55	T2	0.7(Ref)		
E3	5.45	5.50	5.55	V1	0°		8°
e	1.27			V2	0°		8°
G	1.90	2.00	2.10	aaa	0.1		



Footprint(Only for reference)

- NOTES.**
 1. DIMENSION AND TOLERANCE CONFORM TO ASME Y14.5M
 2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH. DIMENSION ARE NOT NECESSARILY EXACT.
 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ween-semi.com>.

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Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

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Date of release: 17 January 2026
