

1. General description

Planar passivated Silicon Controlled Rectifier in a TO247 plastic package intended for use in applications requiring very high inrush current capability and high thermal cycling performance.

2. Features and benefits

- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- High voltage capability
- High di/dt capability
- Very high current surge capability

3. Applications

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control
- Solid State Relay (SSR)
- Traction battery charging

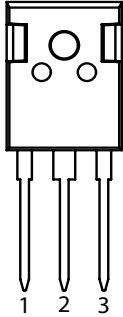

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Notes	Values			Unit
V_{DRM}	repetitive peak off-state voltage			800			V
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 132\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3		80			A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5		800			A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$		880			A
T_j	operating junction temperature			-40 to 150			°C
Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 7		-	-	50	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9		-	-	100	mA
V_T	on-state voltage	$I_T = 80\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10		-	-	1.6	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 150\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit		2000	-	-	V/ μ s

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
TYN80W-800T	TO247	TYN80W-800TQ	Tube	30	TO247N	20-Jul-2016

7. Marking

Table 4. Marking codes

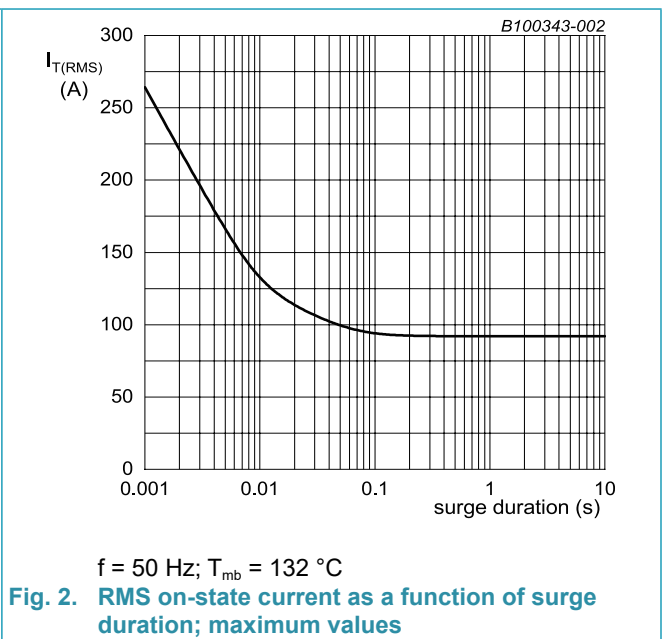
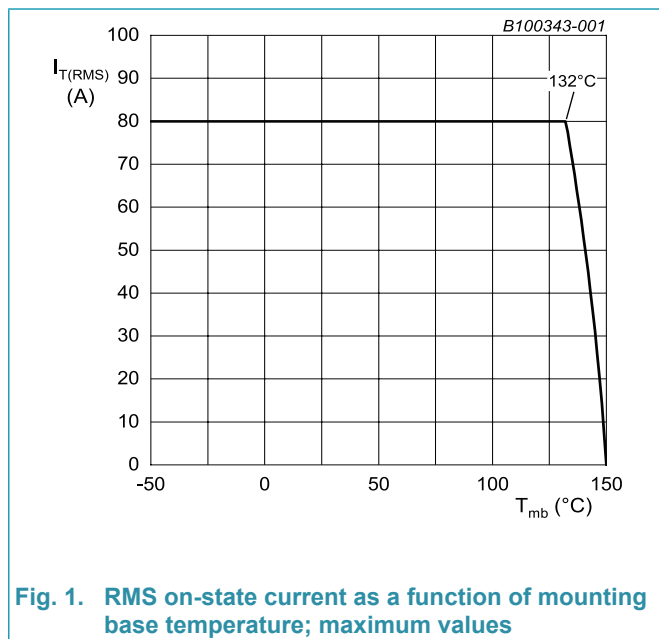
Type number	Marking codes
TYN80W-800T	TYN80W 800T

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DRM}	repetitive peak off-state voltage			800	V
V_{RRM}	repetitive peak reverse voltage			800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 132\text{ °C}$;		51	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 132\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3		80	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5		800	A
		half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$		880	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN		3200	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 100\text{ mA}$		500	$A/\mu s$
I_{GM}	peak gate current	$t_p = 20\text{ }\mu s$		5	A
V_{GM}	peak gate voltage	$t_p = 20\text{ }\mu s$		5	V
P_{GM}	peak gate power			20	W
$P_{G(AV)}$	average gate power	over any 20 ms period		0.5	W
T_{stg}	storage temperature			-40 to 150	$^{\circ}C$
T_j	operating junction temperature			-40 to 150	$^{\circ}C$



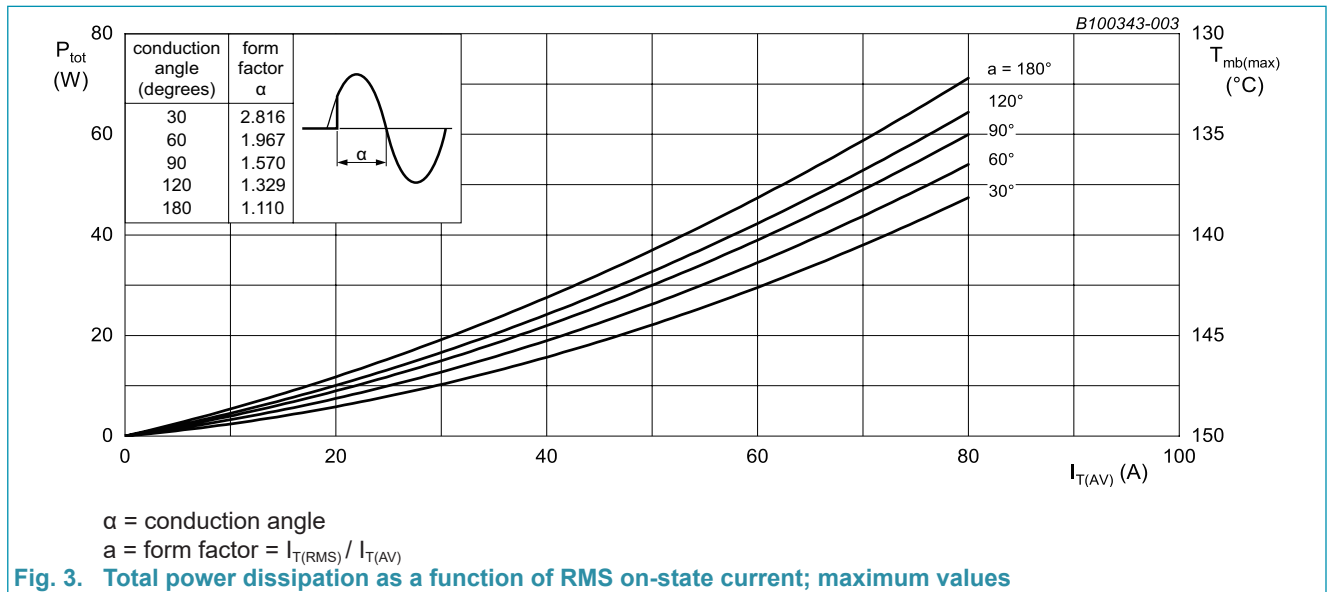


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

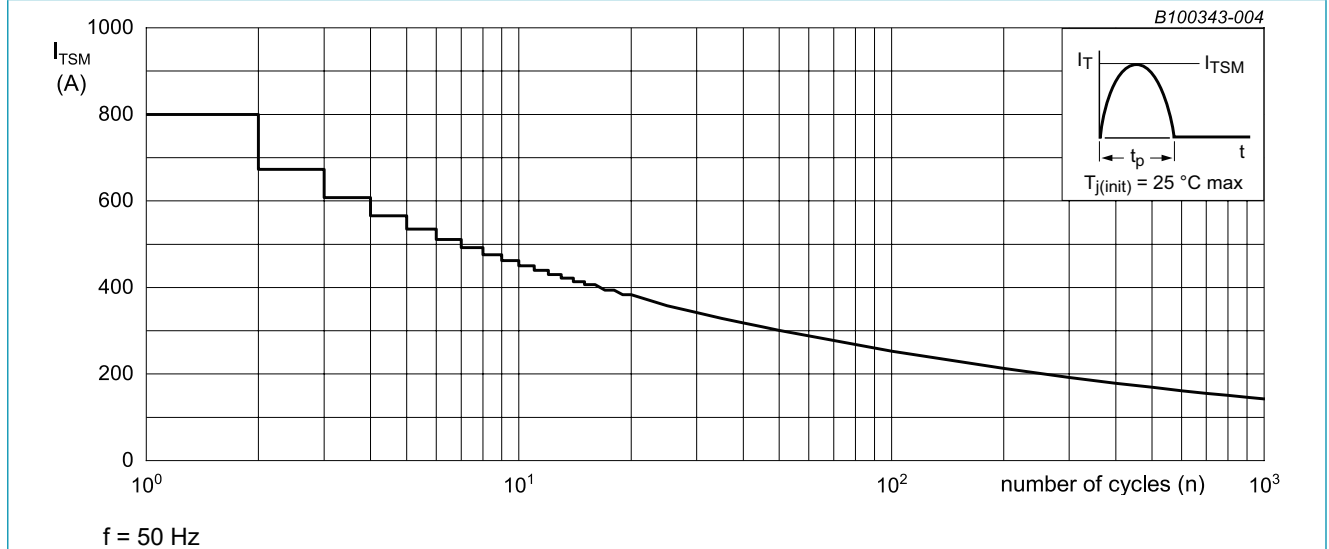


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

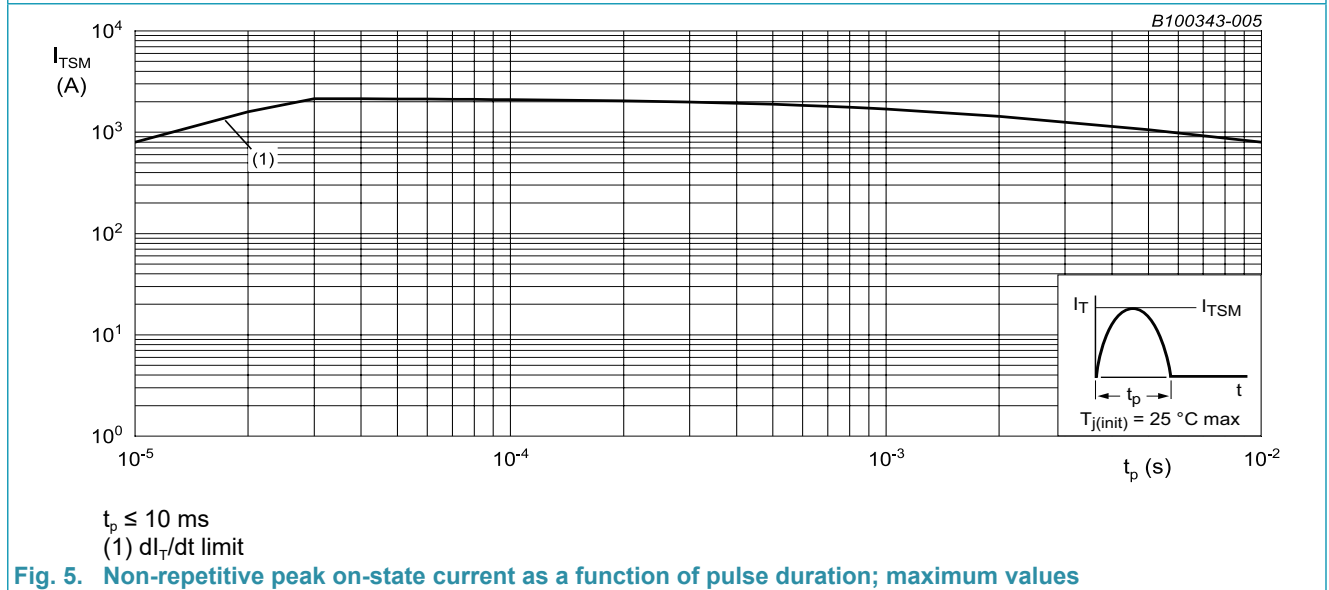


Fig. 5. Non-repetitive peak on-state current as a function of pulse duration; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 6		-	-	0.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	50	-	K/W

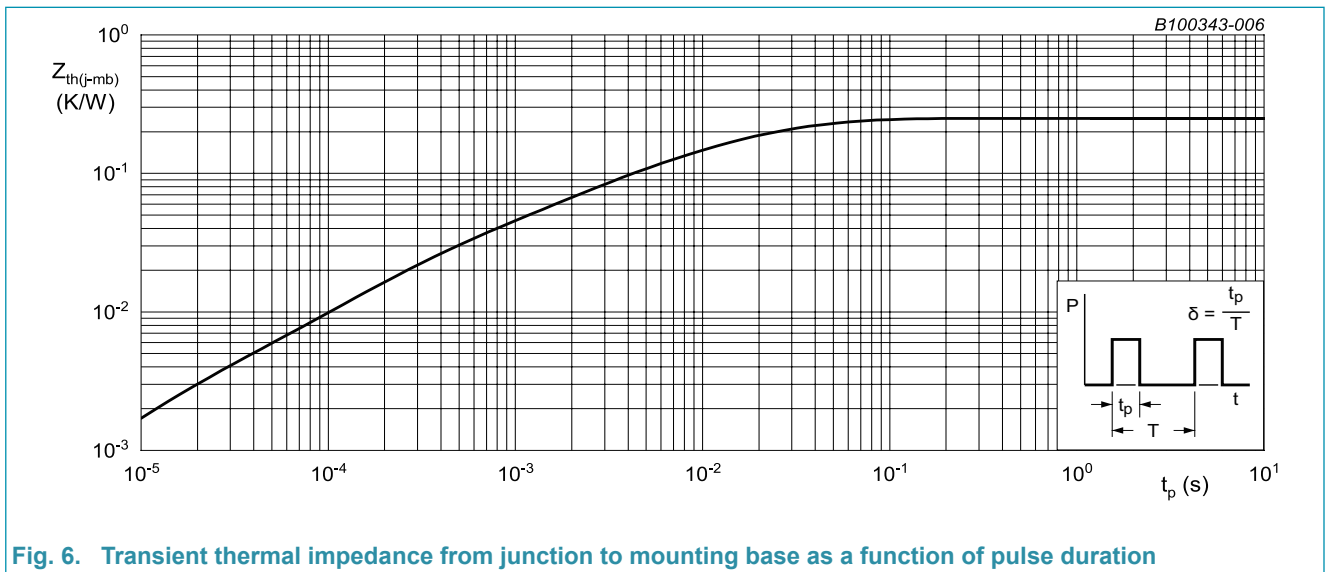
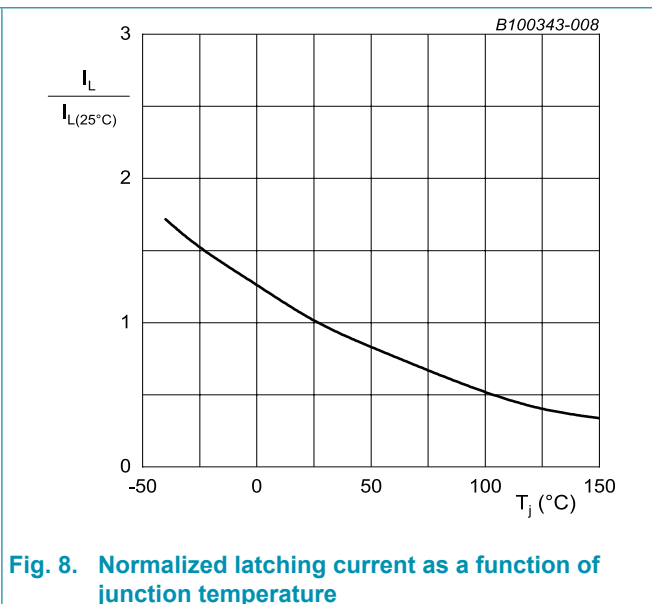
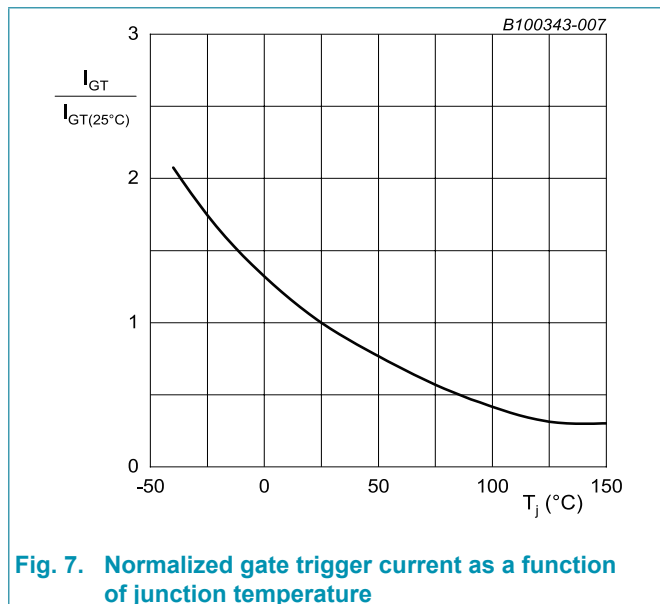


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 7		-	-	50	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 8		-	-	120	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9		-	-	100	mA
V_T	on-state voltage	$I_T = 80\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10		-	-	1.6	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		-	0.7	1.0	V
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 150\text{ °C}$		0.25	0.40	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 25\text{ °C}$		-	-	10	μA
		$V_D = 800\text{ V}$; $T_j = 150\text{ °C}$		-	-	2	mA
I_R	reverse current	$V_R = 800\text{ V}$; $T_j = 25\text{ °C}$		-	-	10	μA
		$V_R = 800\text{ V}$; $T_j = 150\text{ °C}$		-	-	2	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 150\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit		2000	-	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 80\text{ A}$; $V_D = 800\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 1\text{ A}/\mu\text{s}$; $T_j = 25\text{ °C}$		-	2	-	μs
t_q	commutated turn-off time	$I_{TM} = 40\text{ A}$; $t_p = 50\text{ }\mu\text{s}$; $dV/dt = 5\text{ V}/\mu\text{s}$; $dI/dt = 30\text{ A}/\mu\text{s}$; $T_j = 25\text{ °C}$		-	70	-	μs



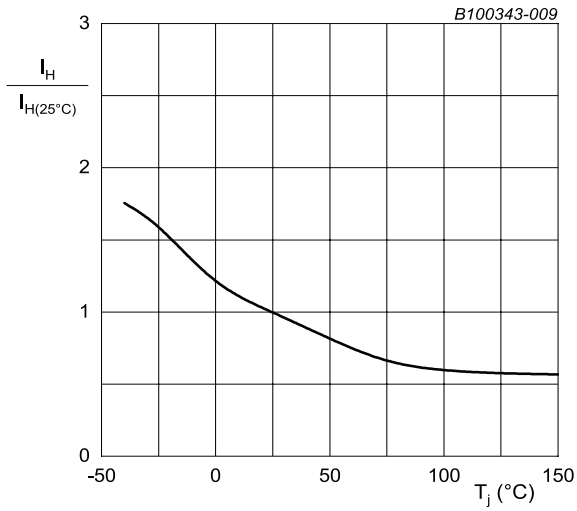
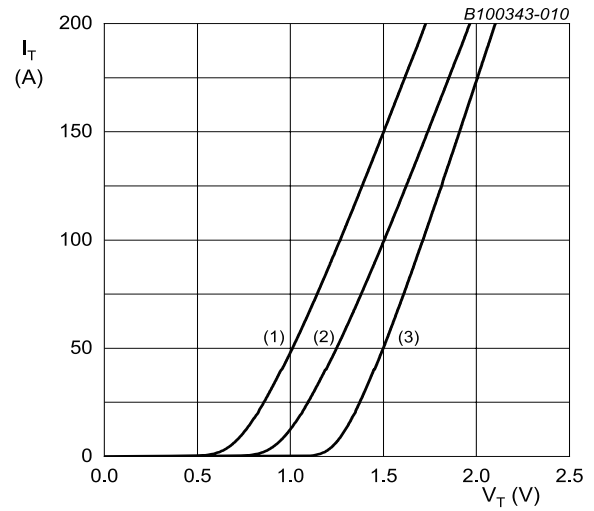


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 0.767 \text{ V}; R_s = 0.0050 \Omega$
 (1) $T_j = 150 \text{ }^\circ\text{C}$; typical values
 (2) $T_j = 150 \text{ }^\circ\text{C}$; maximum values
 (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

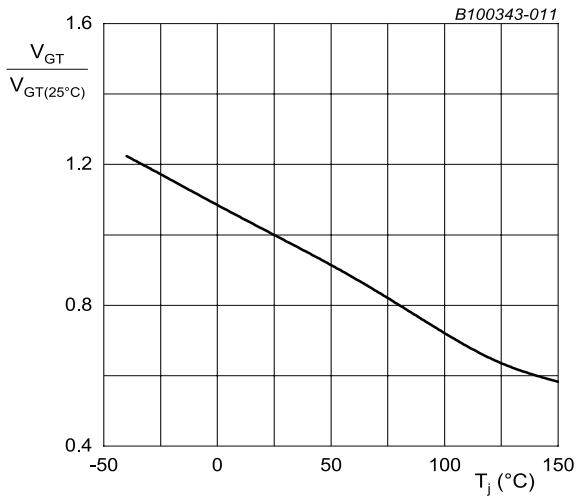
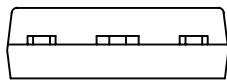
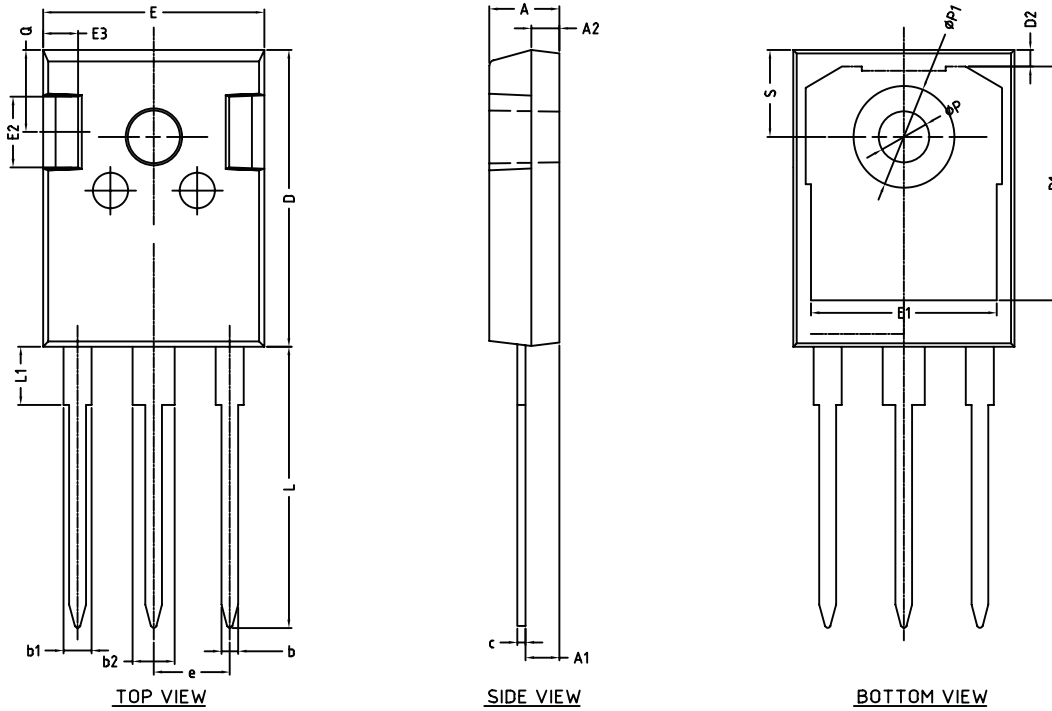


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247

SOT429N



SIDE VIEW

UNIT	A	A1	A2	b	b1	b2	c	D	D1	D2	E	E1	E2	E3	e	L	L1	P	P1	Q	S
mm	MAX	5.20	2.60	2.10	1.40	2.20	3.20	0.70	21.10	16.85	1.35	15.90	13.50	5.20	2.60	20.10	4.75	3.70	7.40	6.00	6.25
	MIN	4.70	2.20	1.90	1.00	1.80	2.80	0.50	20.90	16.25	1.05	15.70	13.10	4.80	2.40	5.45	19.80	-	3.50	-	5.60

OUTLINE VERSION	REFERENCES				PROJECTION	ISSUE DATE
	IEC	JEDEC	EIA J			
SOT429N		TO-247				

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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