WAT120TBS12

SCR Module

Rev.03 - 17 November 2026 Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) module in WeEnTOP-B for use in applications requiring high blocking voltage capability, high inrush current capability and high thermal cycling performance.

2. Features and benefits

- Planar passivated thyristor chips for voltage ruggedness and reliability
- Top-side cooling
- Compact design
- One screw mounting
- Heat transfer and isolation through direct copper bonded aluminum oxide ceramic (DBC)
- Package is RoHS compliant

3. Applications

- Soft starters
- UPS
- Temperature control
- Lighting control
- AC power control

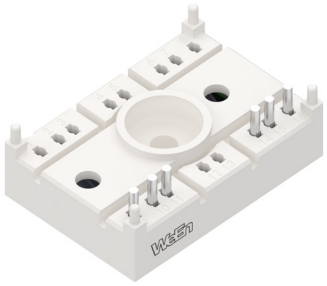
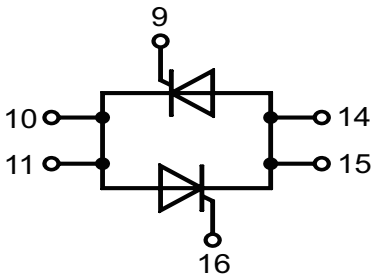
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Notes	Values			Unit
Absolute maximum rating							
V_{DRM}	repetitive peak forward voltage			1200			V
V_{RRM}	repetitive peak reverse voltage			1200			V
$I_{T(RMS)}$	RMS on-state current	half sine wave		134			A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms		2000			A
		half sine wave; $T_{j(init)}$ = 125 °C; t_p = 10 ms		1800			A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		2200			A
		half sine wave; $T_{j(init)}$ = 125 °C; t_p = 8.3 ms		1870			A
Symbol	**Parameter**	**Conditions**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C		30	-	100	mA
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C		-	-	1.50	V
V_T	on-state voltage	I_T = 240 A; T_j = 25 °C		-	-	1.70	V

5. Pinning information

Table 2. Pinning information

Simplified outline	Graphic symbol
	

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
WAT120TBS12	WeEnTOP-B	WAT120TBS12T	Blister	30	WeEnTOP-BPAT-A	05-Nov-2024

7. Marking

Table 4. Marking codes

Type number	Marking codes
WAT120TBS12	WAT120TBS12

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DRM}	repetitive peak forward voltage			1200	V
V_{RRM}	repetitive peak reverse voltage			1200	V
$I_{T(RMS)}$	RMS on-state current	half sine wave		134	A
I_{TSM}	non-repetitive peak onstate current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms		2000	A
		half sine wave; $T_{j(init)}$ = 125 °C; t_p = 10 ms		1800	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		2200	A
		half sine wave; $T_{j(init)}$ = 125 °C; t_p = 8.3 ms		1870	A
I^2t	I^2t for fusing	t_p = 10 ms; sine-wave pulse		20	kA²s
dI_T/dt	rate of rise of on-state current	I_G = 200 mA; T_j = 125 °C		200	A/µs
I_{GM}	peak gate current			10	A
V_{RGM}	peak reverse gate voltage			5	V
P_{GM}	peak gate power			20	W
$P_{G(AV)}$	average gate power	over any 20 ms period		0.5	W
T_{vj}	virtual junction temperature			-40 to 150	°C
T_{stg}	storage temperature			-40 to 150	°C

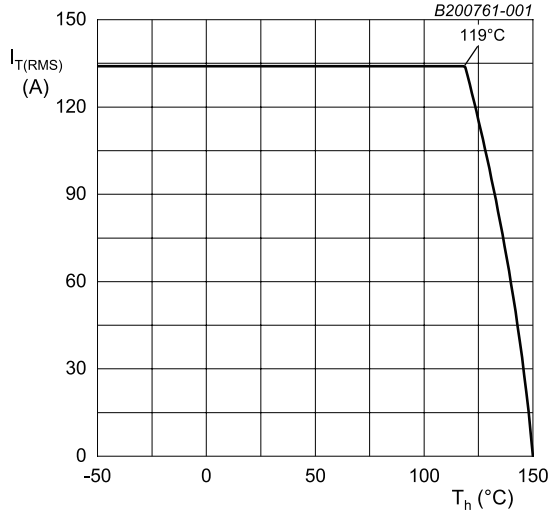
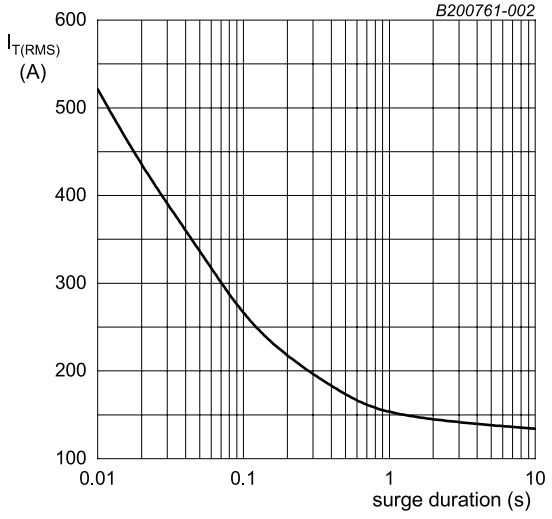


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values



f = 50 Hz; T_h = 119 °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values

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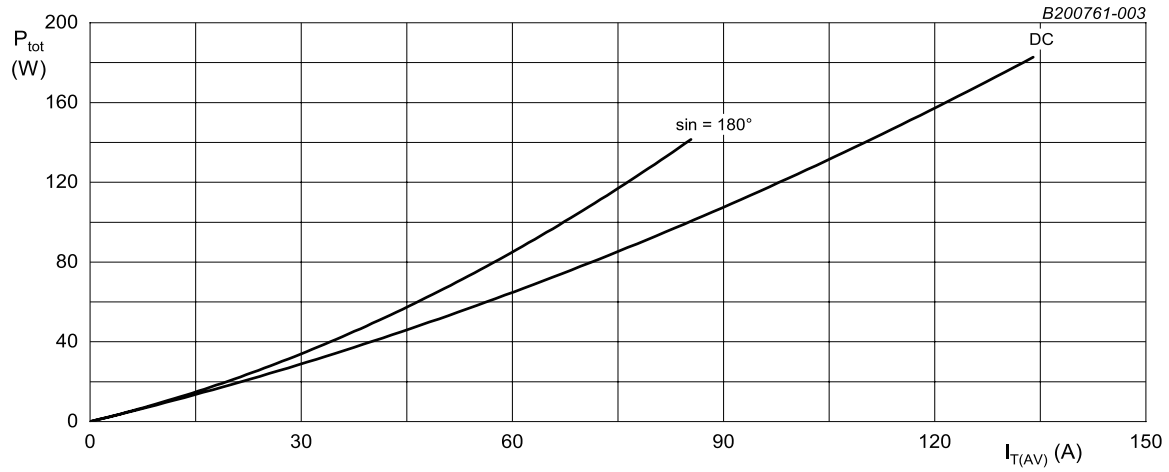
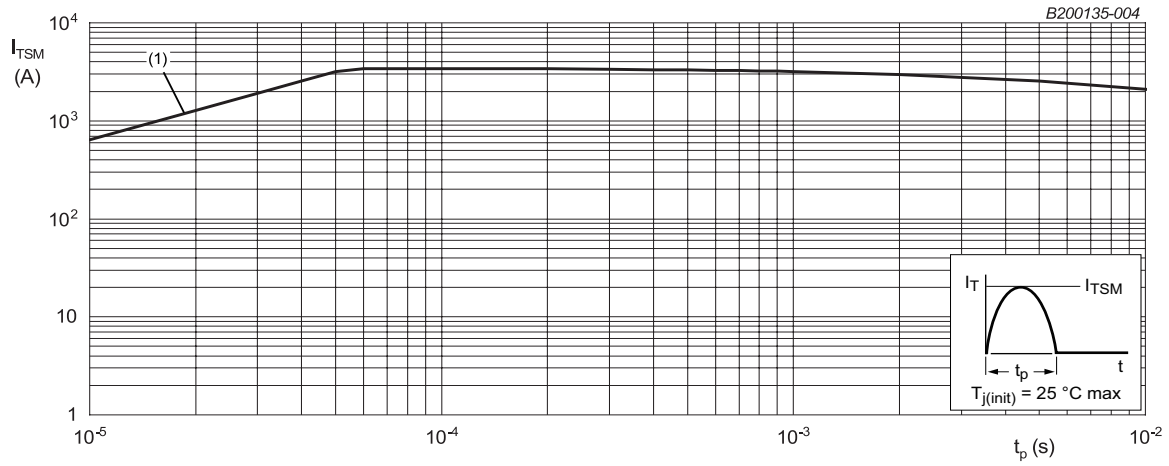


Fig. 3. Total power dissipation as a function of average on-state current; maximum values



$t_p \leq 10$ ms

(1) dI_T/dt limit

Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	per thyristor		-	-	0.44	K/W
		per module		-	-	0.22	K/W

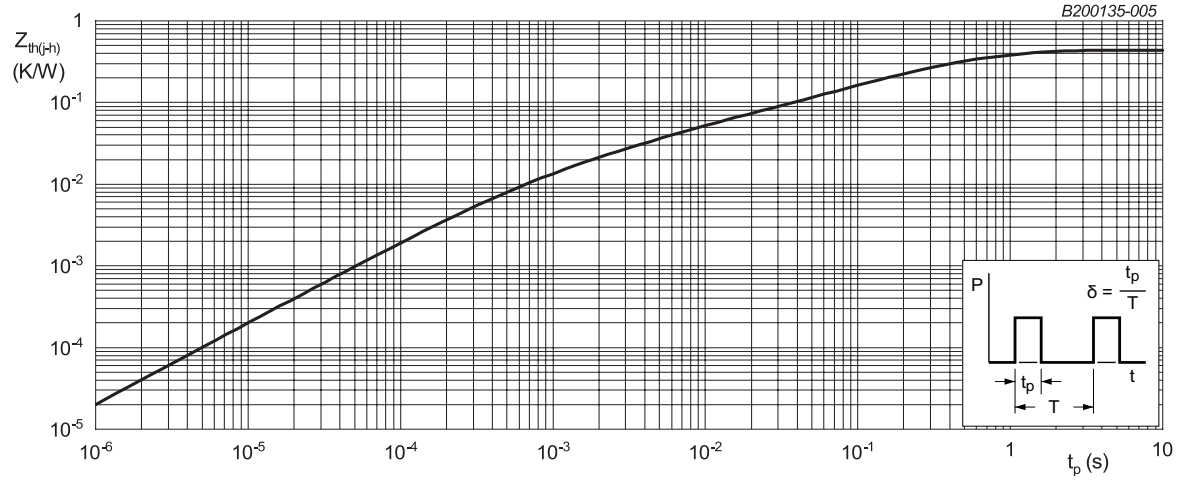

Fig. 5. Transient thermal impedance from junction to heatsink as a function of pulse duration; per thyristor

10. Package characteristics

Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
V_{isol}	isolation voltage	50/60 Hz; RMS; $I_{ISOL} \leq 1$ mA; t = 1 second; AC		-	-	3600	V
		50/60 Hz; RMS; $I_{ISOL} \leq 1$ mA; t = 1 minute; AC		-	-	2500	V

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11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C		30	-	100	mA
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C		-	-	1.50	V
		V_D = 2/3 V_{DRM}; I_T = 0.1 A; T_j = 125 °C		0.25	-	-	V
I_{GD}	gate non-trigger current	T_j = 125 °C		-	-	8.5	mA
V_{GD}	gate non-trigger voltage	T_j = 125 °C		-	-	0.2	V
I_L	latching current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C		-	-	300	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C		-	-	200	mA
V_T	on-state voltage	I_T = 240 A; T_j = 25 °C		-	-	1.70	V
V_{TO}	threshold voltage	T_j = 150 °C		-	-	0.85	V
r_T	slope resistance	T_j = 150 °C		-	-	3.8	mΩ
I_D	off-state current	V_D = 1200 V; T_j = 25 °C		-	-	100	µA
		V_D = 1200 V; T_j = 125 °C		-	-	15	mA
I_R	reverse current	V_R = 1200 V; T_j = 25 °C		-	-	100	µA
		V_R = 1200 V; T_j = 125 °C		-	-	15	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 804 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		1500	-	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 800 V; I_G = 100 mA; $(dI_G/dt)_M$ = 1 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	I_{TM} = 2 A; dV/dt = 5 V/µs; dI/dt = 30 A/µs; T_j = 25 °C		-	50	-	µs

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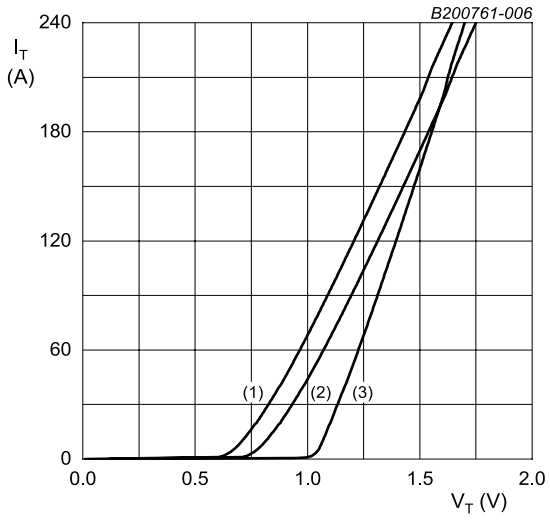

V_{TO} = 0.849 V; r_T = 0.0038 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 6. On-state current as a function of on-state voltage

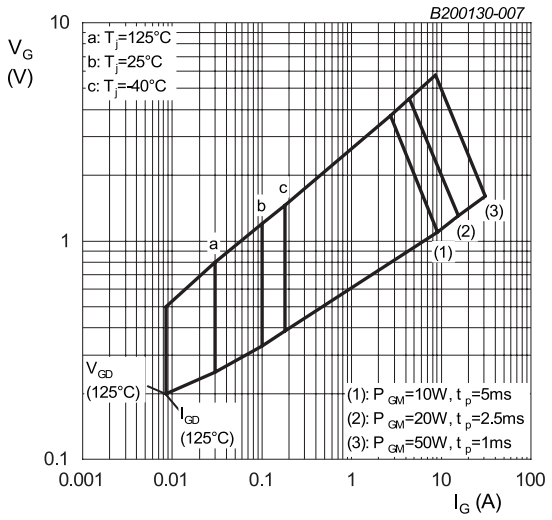

Fig. 7. Gate voltage as a function of gate current

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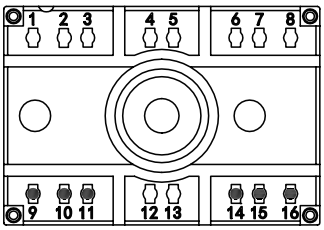
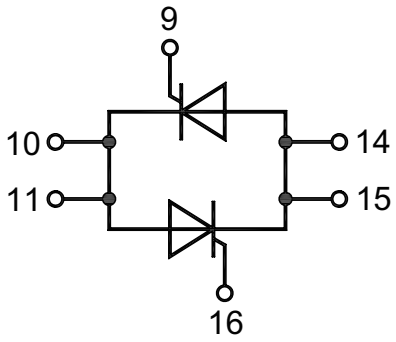
12. Package outline

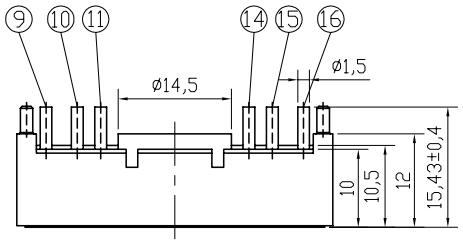
Dimensions in mm

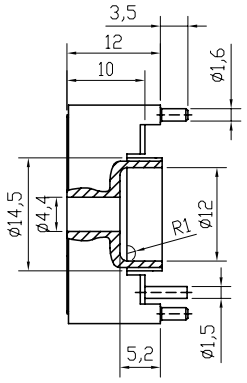
Pinout

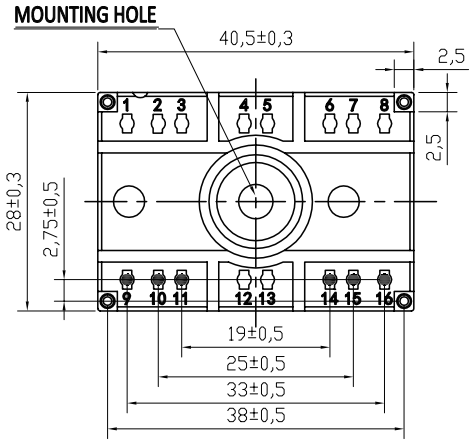




Package Outline







Suggested hole diameter in the PCB for solder pins and mounting pins: 2mm

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